FAA-RD-74-185

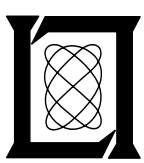
Project Report
ATC-39

Improved MTI Radar Signal Processor

W. H. Drury

3 April 1975

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS



Prepared for the Federal Aviation Administration,
Washington, D.C. 20591

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
FAA-RD-74-185		

4. Title and Subtitle	5. Report Date
Improved MTI Radar Signal Processor	3 April 1975
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
W. H. Drury	ATC-39
9. Performing Organization Name and Address	10. Work Unit No. (TRAIS)
Massachusetts Institute of Technology Lincoln Laboratory P. O. Box 73 Lexington, Massachusetts 02173	11. Contract or Grant No. IAG-DOT-FA72WAI-242
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Project Report
Department of Transportation Federal Aviation Administration Systems Research and Development Service Washington, D. C. 20591	14. Sponsoring Agency Code

15. Supplementary Notes

This work was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology under Air Force Contract F19628-73-C-0002.

16. Abstract

A new type of radar digital signal processor for use with ASR radars is described. It features spectral processing accomplished by combining a 3-pulse canceller with an 8-point, weighted, discrete Fourier transform and adaptive thresholds. This combination of circuits provides a 20-dB increase in MTI improvement factor over present ASR's and is within 2 dB of optimum processing results. An auxiliary channel is provided to allow detection of any target traveling tangentially if its return exceeds the level of ground clutter return in the occupied range/azimuth cell. The spectral processing technique provides discrimination against weather clutter if the returns from weather and from the target fall into different Doppler frequency regions.

The output from this equipment is digital hit reports for transmittal to the ARTS-III IOP computer.

17. Key Words	18. Distribution Statement
Airport Surveillance Radar (ASR) Radar MTI Clutter Doppler Processing	Document is available to the public through the National Technical Information Service, Springfield, Virginia 22151.

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	
Unclassified	Unclassified	92	

TABLE OF CONTENTS

I. INTRODUCTION

The Moving Target Detector system (MTD) is a signal processor to improve the performance of Airport Surveillance Radars (ASR's). It features spectral processing with adaptive thresholds and thereby provides a 20 dB increase in signal improvement factor over the present ASR's. An auxiliary channel is included to allow detection of any target traveling tangentially if its return exceeds the level of ground clutter return in the specific range/azimuth cell occupied. The spectral processing technique provides discrimination against weather clutter if the returns from weather fall into frequency regions which do not include the target returns.

The system parameters are:

Transmitter pulse width	1 μsec.
Pulse repetition frequency	
Pair "A"	1.1131 kHz 1.3677 kHz
Pair "B"	1.1208 kHz 1.3794 kHz
Pulses per Coherent Processing Interval (CPI)	10
CPI's per antenna scan	480
Range gate length	1/16 mi
Range coverage	47.5 mi
Azimuth coverage	360^{o}
Azimuth resolution	0.75^{o}
Antenna beamwidth (two-way)	1^{o}
Sensitivity Time Control (STC) curve	varies as $(\text{range})^{-4}$

The prf alternates from CPI to CPI in order to resolve Doppler ambiguities, and changes between "A" and "B" pairs on alternate scans to identify second-time-around range returns.

II. BLOCK DIAGRAM DISCUSSION

Figure 1 is a system gross block diagram. This discussion will treat each block in turn.

A. Timing

The timing portion of the MTD accepts antenna position information and the 30.9875 MHz master oscillator signal and outputs all the necessary triggers and pulses which are radar related. The signals used for timing within the latter stages of the processor are generated by the DFT control unit to be described later.

The outputs are:

- Azimuth change pulse
- Azimuth reference pulse
- Azimuth data word
- Transmitter pre-trigger
- 31 MHz pulse to exciter
- Zero range trigger
- End sweep time trigger
- Encode commands for A/D converters
- Operator selected range gate sampler
- Start CPI
- End CPI
- STC attenuation word
- H. V. power supply regulator control gate

There are also several signals output which are generated by combining one or more of the above.

B. Input Processing

The Computer Labs model 5103 A/D converters that are used to digitize the quadrature video are capable of converting each 335 nsec, although the range

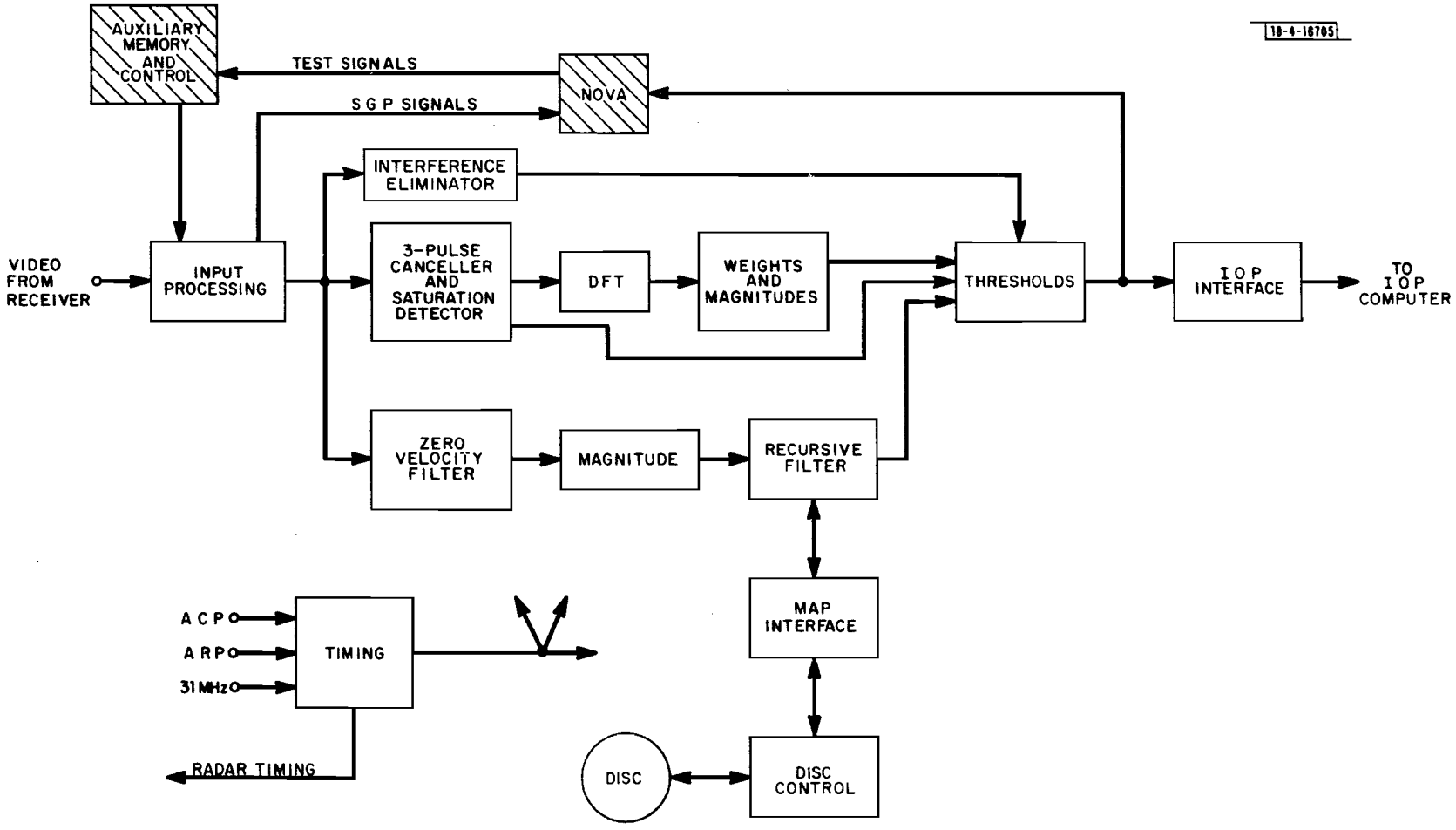


Figure 1 - MTD Block Diagram

interval of the radar is 775 nsec (1/16 mile). To take any possible advantage of this fact, two samples are taken during each range gate and the results added together. Thus, with 10-bit converters, we present an 11-bit sample to the input of the processor.

Since spectral analysis with an 8-point discrete Fourier transform requires eight samples of the input wave and two pulses are required to "charge up" the 3-pulse canceller, the system must gather ten samples of an input signal before processing can be started.

A core memory is used to store data from ten radar sweeps of 760 range gates each. The processing can then begin by putting the ten samples from the first range gate into the canceller. These are followed by the ten samples of the second gate, etc.

The addressing for the 8K core memory is such that each cell is filled with new data as soon as it has been read out. In this way, only 7600 words of storage are required.

A set of switches is provided to allow selection of one particular range gate of the 760. The digitized video from this selected gate is fed to the NOVA computer for use in the Single Gate Processor (SGP) program. The SGP is not required for normal operation and is only used as a diagnostic tool to examine the stability of various parts of the radar.

C. Saturation Detector and Interference Eliminator

Since the system processes ten signal samples as a unit, it must remember and discard an output formed from an input set where any sample

saturated the A/D converter. For simplification of hardware, saturation is defined as 0.5 dB below converter limits. Interference from other radars in the vicinity appears as one large return in the series of ten, unless the radar is synchronous with the FPS-18 radar, which is unlikely. The interference eliminator compares the magnitude of each pulse of the ten against the average magnitude of the ten. If any pulse is greater than five times the average, all information from that range/azimuth cell is discarded.

D. Three-Pulse Canceller

The output of the 8K core memory feeds the canceller and zero velocity filter (ZVF) as well as the saturation detector. The canceller uses the algorithm a-2b+c where, a, b and c are three consecutive samples. Since coherent processing intervals (CPI's) alternate in pulse repetition frequency, the output of the canceller is meaningless until the third sample of a CPI has been accepted. Only the last eight of the ten numbers output from the canceller are passed on to subsequent circuits.

E. Zero Velocity Filter

The canceller not only masks clutter but also prevents the observation of targets traveling at radial velocities near zero or multiples of the prf. Since many range/azimuth cells will exhibit very low, if any, clutter returns, it is a waste to discard them all. The implementation of the zero velocity filter (ZVF) allows detection of any target at low velocity whose return exceeds the level of clutter in that particular cell. Since most ground clutter is of a fixed nature, the system uses a disc memory to "remember" the clutter level in every cell from scan to scan, thereby providing a reference to threshold new signals against.

F. Discrete Fourier Transform

The MTD uses an 8-point discrete Fourier transform (DFT) implemented by the fast Fourier transform (FFT) algorithm. The hardware uses no multiplies except by powers of two (shifts) to compute the transform. The only fraction, $1/\sqrt{2}$, is approximated by the sum $1/2 + 1/8 + 1/16 + 1/64 + 1/256$ which is all implemented by shifts and carrys. The DFT is made up of an arithmetic unit, a scratch-pad memory and a controller containing a hard-wired program of 80 instructions. This controller provides the timing pulses for the DFT and all subsequent portions of the MTD. The input to the DFT is eight samples in time of each of 760 range gates while the output is the response of eight digital filters presented sequentially for each of the 760 gates.

G. Weighting and Magnituding

The DFT output is weighted by using the algorithm that each filter output is diminished by 1/4 the value of each of the two adjacent filters. For this purpose the zeroth filter is adjacent to the seventh filter. The weighted signals are then fed to a magnitude-taking circuit which uses the algorithm M = greater of: $|L|, \{ 7/8\ |L| + 1/2\ |S| \}$ where L and S are the larger and smaller of the I and Q components of the signal. It can be shown that this diverges from $\sqrt{I^2 + Q^2}$ in the worst case by less than 0.2 dB.

At the input of the magnituder, the output from the ZVF is substituted into the time-slot of the zeroth DFT filter, since the zeroth filter has had all DC removed by the canceller.

H. Thresholds

Separate thresholding takes place on each filter output. The thresholds for the non-zero filters are based on the average returns in that filter for a one-mile range interval centered on the cell of interest. The threshold for the ZVF is based on the past history over many minutes of the returns in the cell of interest. These two concepts of thresholding were chosen because of the character of ground and weather clutter. Weather clutter will generally be dispersed in range over several cells, whereas ground clutter is quite independent from cell to cell. On the other hand, weather clutter is quite time-varying, but ground clutter in a given cell remains relatively constant in level over long periods of time. The problem of storing ground clutter information for each of 365,000 range/azimuth cells is solved by using a disc memory unit. However, the asynchronism between the radar and the disc and the relatively long access time of the disc requires that some 3,000 words must be buffered into and out of the disc memory. This is accomplished by using MOS shift registers. If the appropriate threshold is exceeded and there were no A/D saturations or interference in the raw data, an output message is entered into the output interface circuitry.

I. Output Interface

The output circuitry contains double buffering for up to 38 detections per CPI. Double buffering is required because the MTD and the Input/Output Processor (IOP) are asynchronous devices. At the start of each CPI, a prf/azimuth (PAZ) word is entered into the first buffer. When a threshold

crossing takes place a velocity/range/strength (VRS) word for that detection is entered into the first buffer. At the end of each CPI the PAZ word and any VRS words for that CPI are transferred from the first to the second buffer. During the next CPI the contents of the second buffer is transferred to the IOP. The NOVA computer is also connected to this output and receives data in parallel with the IOP.

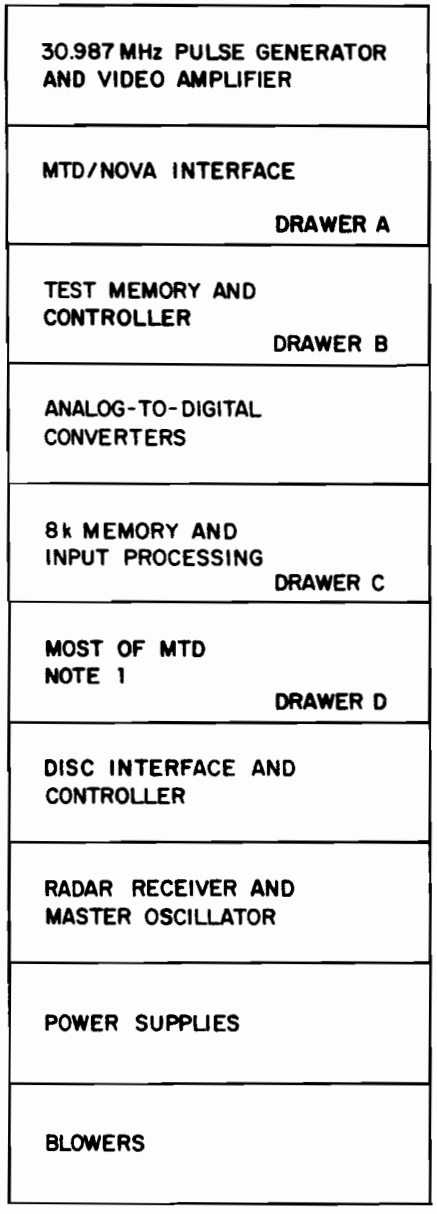
J. MTI Weather Video Output (Not required for automatic operation)

In most cases, it is useful for the operator to be able to see the location of storms on his display screen. Since the MTD does an excellent job of eliminating the radar returns from bad weather, an ancillary channel was added to form such a signal. The returns from all non-zero filter outputs are added together at the magnituder output and then averaged over three range gates, thus forming 254 outputs in range for each CPI. A 256 word memory is used to store these numbers and is read out to the display each sweep. As each piece of new information is generated it is stored in the proper cell of the memory, replacing the previous value for that cell.

K. Auxiliary Memory (Required only for testing purposes)

A core memory is supplied which can be connected to the input of the MTD in place of the A/D converters for testing. This memory can be loaded with 7,600 words (a full CPI) of known input data. The MTD will then process this data with identical and predictable results in each CPI, thus making it easy to observe processor faults.

Figure 2 is a diagram of the physical layout of the MTD rack and Figure 3 is a diagram showing the layout of the inter-chassis cabling.



NOTE 1

CONTENTS OF DRAWER D

(a) 3-PULSE CANCELLER
(b) SATURATION DETECTOR
(c) INTERFERENCE ELIMINATOR
(d) ZERO VELOCITY FILTER
(e) DFT AND CONTROL
(f) WEIGHTING
(g) MAGNITUDING
(h) THRESHOLD GENERATORS
(i) THRESHOLD CROSSING DETECTOR
(j) TIMING
(k) OUTPUT INTERFACE
(l) ALL ADJUSTMENTS

Figure 2 - MTD Physical Configuration

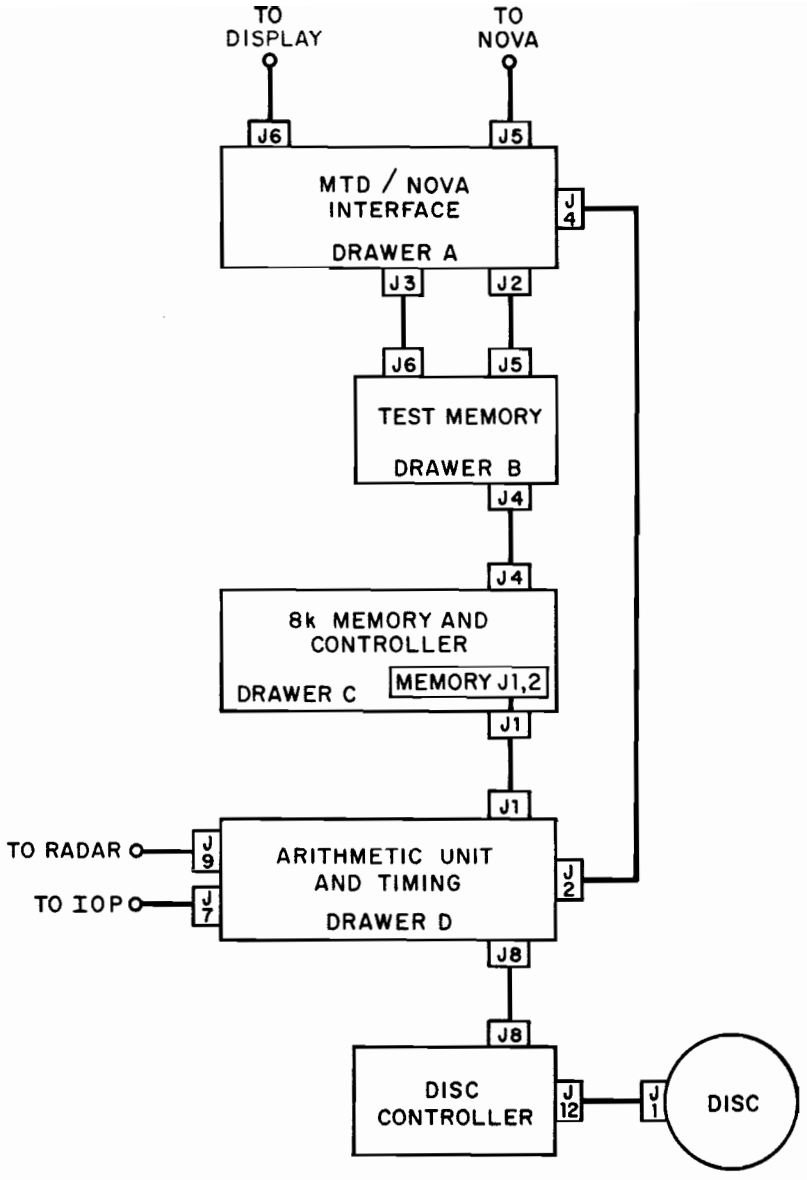


Figure 3 - MTD Cabling Diagram

III. TIMING

The timing shown by the block diagram of Figure 4 can be logically divided into four sections:

1. Generation of the pulse repetition frequency (prf) for the radar.
2. Signals generated each prf.
3. Fast timing.
4. Selected range gate.

The entire timing section is located in the top rear panel of drawer "D".

A. PRF Generation - Theory

The prf is generated in bursts of ten pulses, two such bursts constituting a CPI pair. The initiation of a CPI pair must depend on antenna position since the use of a clutter map dictates that CPI's be correlated with azimuth. In the $\approx$4.8 seconds that it takes for one revolution of the antenna, 240 CPI pairs are generated. Azimuth change pulses (ACP's) are generated by the antenna at the rate of 4096 per revolution. In order that the CPI's be distributed as equally as possible in azimuth, a CPI pair is initiated each 17 ACP's. Simple calculation reveals that 240 CPI pairs will be generated in less than 4096 ACP times, so each 15th CPI pair is initiated after 18 ACP's rather than 17. This distributes the error through the entire scan.

During the period of 17 ACP's the transmitter must be triggered at one prf ten times, at a second prf ten times and at an average of the two prf's as many times as necessary to fill the rest of the interval. This last number may be any number from one to about four because the antenna speed changes slightly with wind loading, causing differences in inter-ACP time. The time filled with average prf must be long enough so that it never goes to zero under worst case antenna speed variation.

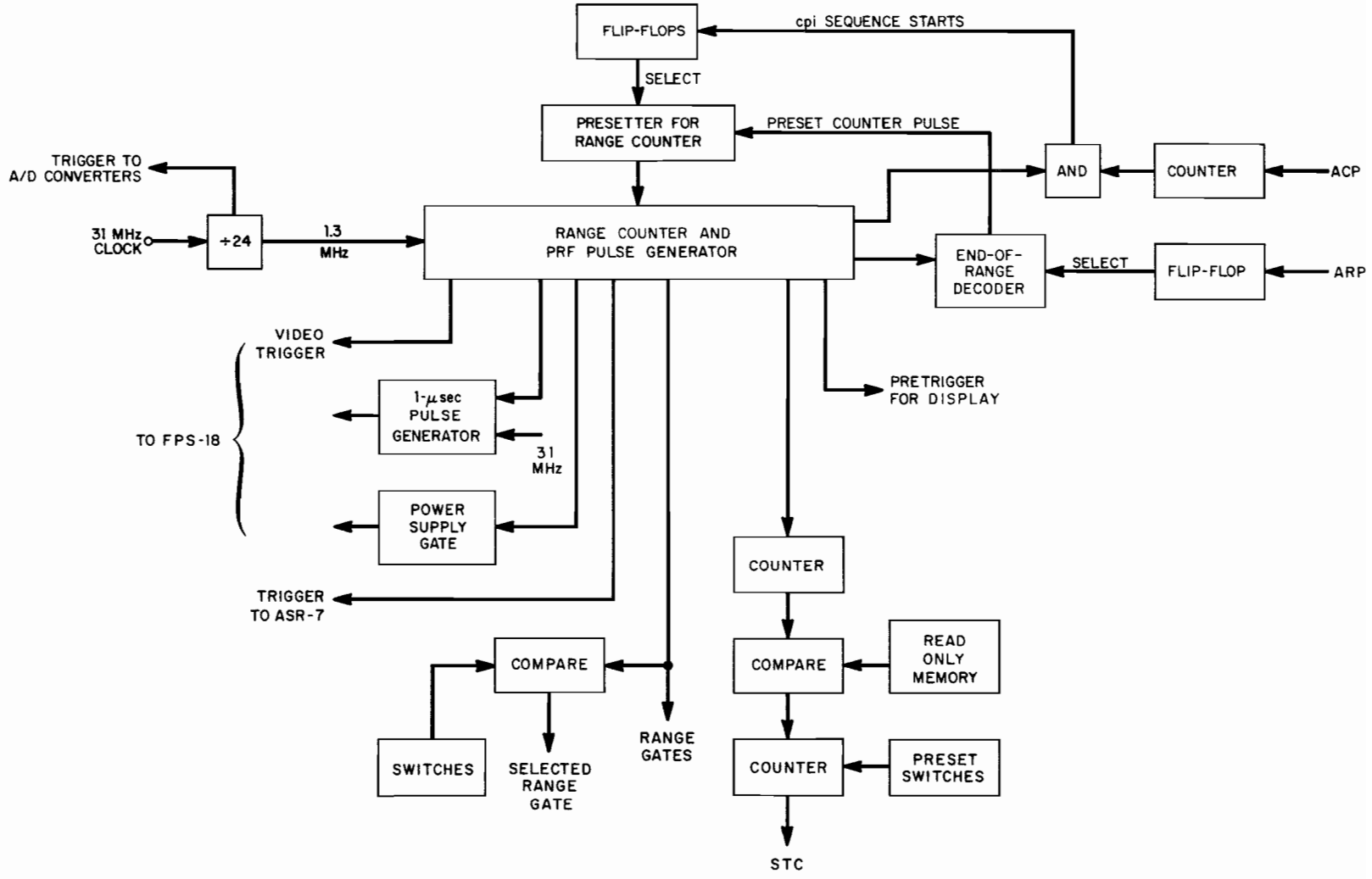


Figure 4 - Timing Block Diagram

During the 17-ACP interval, a range counter is counting at a 1.3 MHz (1/16 mile) rate up to the end-of-range trigger. When that point is reached the counter jumps to a negative number, shown by point B in Figure 5 and continues counting up through zero range and to the next end-of-range time. End range times D and E on Figure 5 are used on alternate scans, providing a slight jitter in prf from scan to scan.

Following recepit of each 17th (or 18th) ACP the jumpback point for the counter is shifted to point A for 10 times, then to point C for 10 times, before reverting to point B. The table in Figure 5 gives a summary of the prf frequencies that are generated by this method.

B. PRF Generation - Details

ACP pulses are routed to a counter whose output feeds a comparitor. The counter is reset to zero by the azimuth reference pulse (ARP) each time the antenna passes through north. The other side of the comparitor is fed from the output of another counter which is incremented in units of 17 counts. (Each 15th time it is incremented by 18 counts.) Incrementing is caused by the occurrence of an output pulse from the comparitor (COMP). In effect, the other side of the comparitor advances 17 (18) counts each time the ACP counter catches up to it.

Video trigger (VTRG), generated near zero range count, is ANDed with COMP to produce a sequence initiate pulse (SEQ). SEQ zeros a counter which counts VTRG pulses. P10 and P20 are counter outputs which are divide-by-10 and divide-by-20, respectively. These are decoded to reset the range counter to the proper number for low, high or average prf.

INTERVAL	NO. COUNTS	μsec	PRF GENERATED (kHz)	
A TO D	1152	892	1.1208	LOW
C TO D	936	725	1.3794	HIGH
B TO D	1040	805	1.2415	AVERAGE
A TO E	1160	898	1.1131	LOW
C TO E	944	731	1.3677	HIGH
B TO E	1048	812	1.2320	AVERAGE

Figure 5 - Timing Diagram

Note that the two CPI's of the pair start at SEQ and P10. These two signals are ORed and then ANDed with a zero range pulse (ZT) to produce start CPI (SCPI). This pulse is also known as load increment (LINC). The first ZT after SCPI is selected also and called set increment (SINC). These last two signals are used in the input processing section and the reason for their names will become obvious when that section is covered. After the 10th cycling of the range counter in a CPI, the end sweep time (EST) pulse is selected and called end CPI (ECPI). A gate is generated between SCPI and ECPI and appropriately identified as the CPI gate.

The ACP counter which was used to generate COMP contains real-time azimuth information. Midway in each CPI, azimuth sample (AZSAM) is decoded which latches the azimuth count into a double buffer. This is necessary because the Fourier transform processing is all performed one CPI late and the azimuth of the past CPI must be remembered. This azimuth word will become part of the output data package.

In the absence of ACP and ARP pulses (such as when the antenna is stopped) an internal generator in the MTD automatically takes over so that the transmitter will continue operating.

C. Signals that Repeat at the PRF

Each pulse repetition interval the range counter counts at 1.3 MHz (1/16 mi) from a preset negative number up through zero count (ZT) to end of sweep time (EST). The counter resets to the negative number at DTT pulse time. The position of DTT changes by eight counts from scan to scan providing a slight jitter. Various triggers are decoded along the way as the counter runs and these are summarized in Table 1. The bits of the counter form real-

TABLE 1

TIMING PULSES GENERATED EACH PULSE REPETITION TIME

Name	Time in Counts	Time in μsecs	Purpose
PT	-129	-100	Display pretrigger
ASRTRG	-31	-24	Coho lock pulse for ASR-7 radar
VTRG	-10	-8	Modulator trigger for FPS-18 and ASR-7
RFTRG	-5	-4	RF trigger for FPS-18 and ASR-7
ZT	0	0	Zero range time, start of sweep
ONEGATE	1	1	Time of first range gate
EST	760	589	Time of last range gate, end sweep
EST+1	761	590	One count after EST
DTT	768 or 776	595 or 601	Reset range counter to starting point
SWGT	extends from ZT to EST		Sweep gate
PSGT	extends from EST to VTRG		HV power supply regulator control signal

time range and are distributed through the system. The sweep gate (SWGT) and power supply control signal (PSGT) are intervals between some of these pulses and are, therefore, included in Table I. PSGT is a function of prf and is used to provide a constant duty cycle to the high voltage power supply of the transmitter.

The sensitivity time control (STC) attenuator in the receiver is driven from a counter in the timing section. This counter is preset at main-bang time to a number selected by switches and is then decremented to zero by a pulse train whose frequency is a function of range time to the minus fourth power. Each pulse in the train is formed by comparing the output of the range counter with a set of range numbers stored in a read-only memory (ROM). As each comparison is successful, the next word, representing the range of the next pulse, is drawn from the ROM and applied to the comparitor. It is expected that for each given radar siting the optimum number for initial attenuation at main-bang time will be determined. This number will thereafter remain fixed.

D. Fast Timing

The fast timing generates all signals that occur more often than once per sweep. The input from the master oscillator (MO) is nominally 31 MHz and is divided by two to yield 15.5 MHz. Commencing at RFTRG, 16 pulses of this frequency are counted to form a nominal 1-μsec gate. The gate is ANDed with the 31 MHz signal to produce a 1-μsec burst of pulses. This burst if filtered to make the pulses sinusoidal, amplified, gated again and sent to the exciter. The

second gating is performed in a balanced mixer and is necessary because leakage through the TTL gate is excessive. The 15.5 MHz train is further divided by 6 to form a 2.6 MHz signal to be used as the encode command for the A/D converters. An additional division by two yields 1.3 MHz, the range counter clock.

E. Selected Range Gate (Required only for testing purposes)

A single range gate (SRG) is selected manually by setting a bank of switches to the desired range. This setting is compared to the range counter output and a pulse generated at the time of coincidence. The output is used to sample and hold the outputs of the A/D converters in that particular range gate for transmission to the NOVA and its SGP spectrum analysis program. A pulse slightly ahead of SRG is used to initiate a second burst of 31 MHz for the exciter. This burst generates a test target in all azimuths at SRG time. A switch is included to prevent generation of this second burst when no test target is desired.

IV. INPUT PROCESSING

The input processing section of the MTD, shown in Figure 6 and located in drawer 'C' can be divided into three sections.

1. Sample combiner
2. Memory and controller
3. SRG pickoff

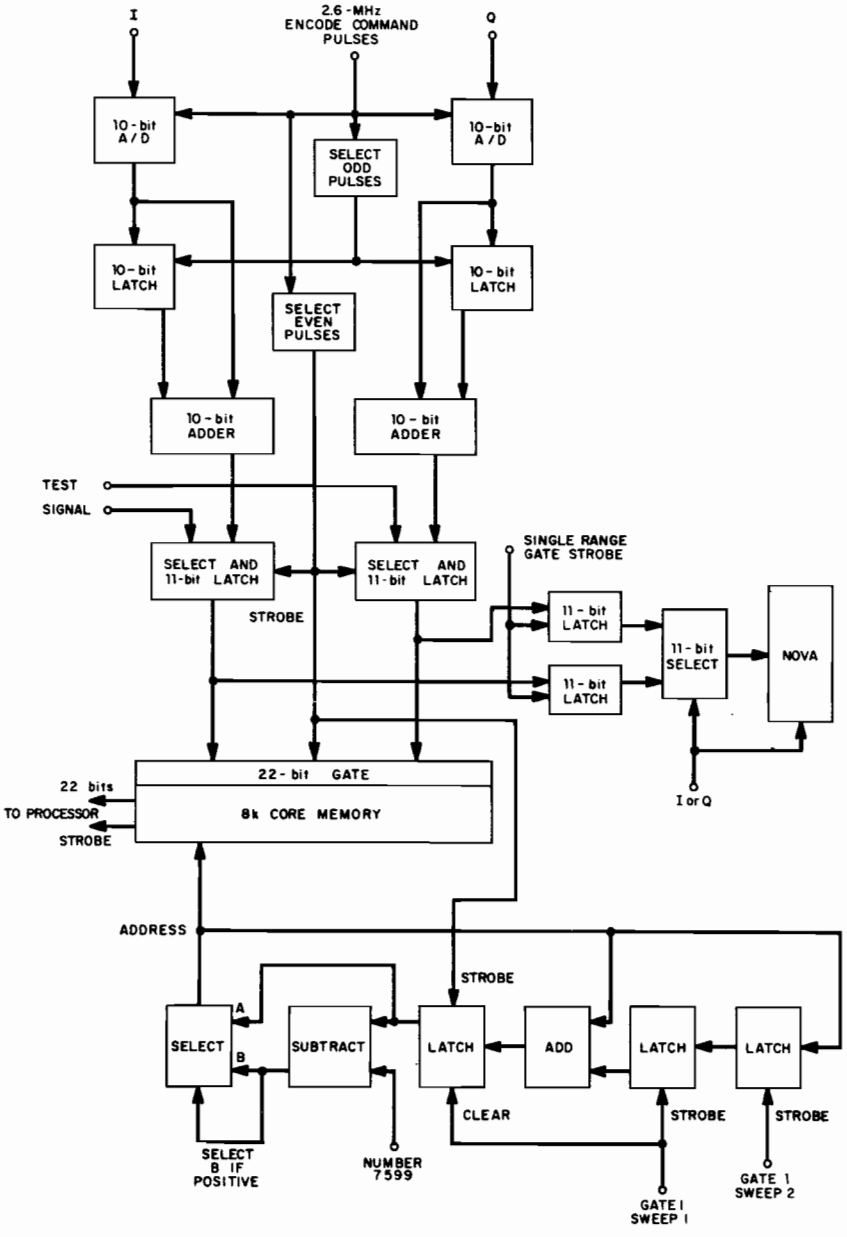


Figure 6 - Input Processing Block Diagram

A. Sample Combiner

Two 10-bit samples are taken in each range gate by the A/D converters on command of the 2.6 MHz clock signal. The first sample of a pair is stored and added to the second to produce a single 11-bit sample in each gate. This sum is then entered into a memory via a selector switch. When this switch is in the TEST position, the sample word is replaced by a word drawn from a "test" memory to be discussed later.

B. Memory and Controller

Since the MTD must process ten samples from the same range gate as a group, there must be storage for ten samples of each of the 760 range gates or 7600 pairs of 11-bit I & Q words. To eliminate the need for "ping-ponging" two memories, split-cycle operation with an intricate addressing system is used. The memory units can perform a read/modify/write operation in 700 nsecs. The addressing is such that each cell is filled with new data as soon as it is emptied, while maintaining the "orthogonality" or "corner-turning" necessary to re-order the input data for processing. The output of the memory then becomes ten consecutive samples of each of the 760 range gates, as opposed to the input which is 760 range samples for each of ten consecutive sweeps. Figure 7 shows why this process is called orthogonality or corner-turning.

The addressing algorithm is shown in Figure 8 for a small memory array. The entire memory is used each CPI, but the order of cell use changes. The

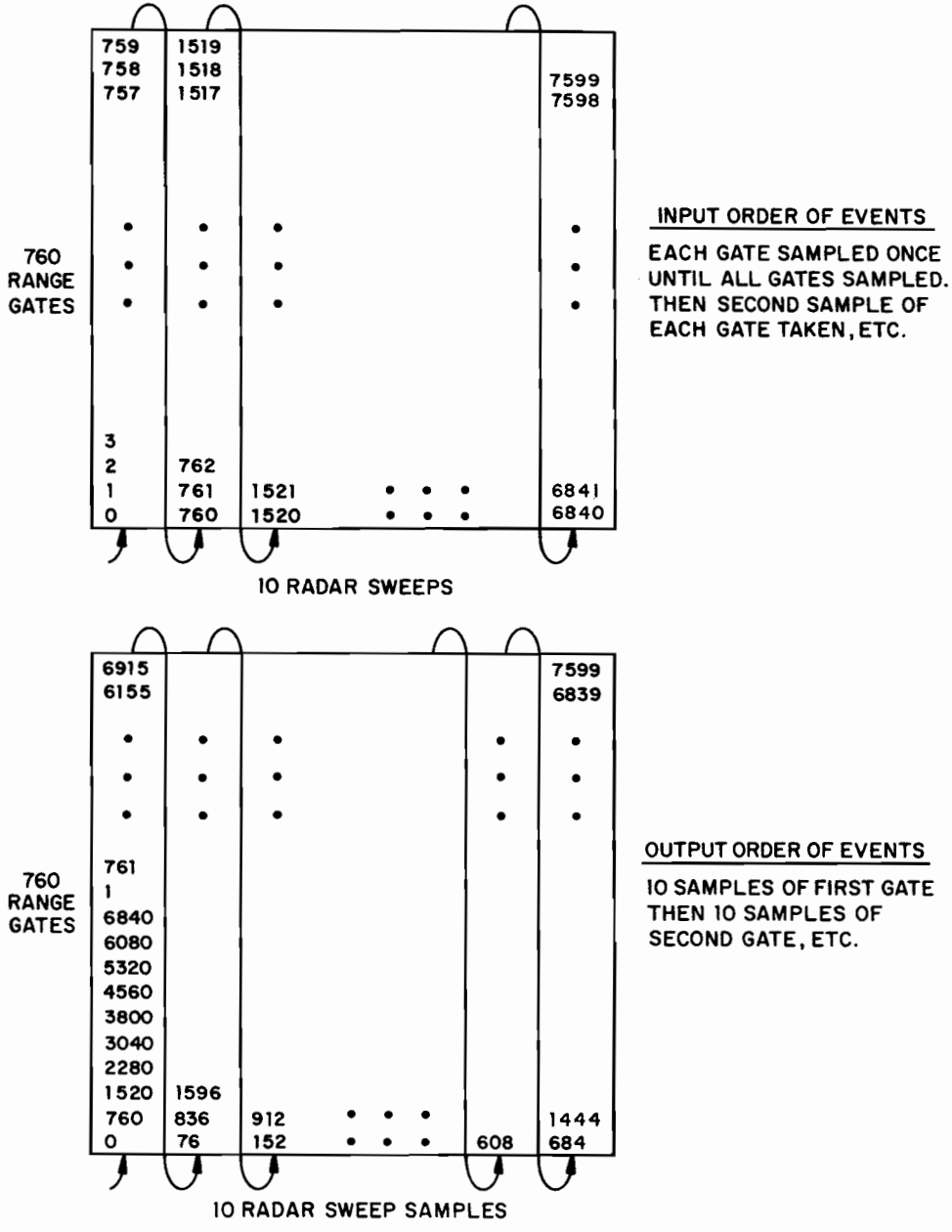


Figure 7 - Input Data Re-ordering

4	9	14	19
3	8	13	18
2	7	12	17
1	6	11	16
0	[5]	10	15

-1-

1	7	13	19
15	2	8	14
10	16	3	9
5	11	17	4
0	[6]	12	18

-2-

5	16	8	19
18	10	2	13
12	4	15	7
6	17	9	1
0	[11]	3	14

-3-

6	4	2	19
14	12	10	8
3	1	18	16
11	9	7	5
0	[17]	15	13

-4-

11	1	10	19
13	3	12	2
15	5	14	4
17	7	16	6
0	[9]	18	8

-5-

17	5	12	19
8	15	3	10
18	6	13	1
9	16	4	11
0	[7]	14	2

-6-

9	6	3	19
2	18	15	12
14	11	8	5
7	4	1	17
0	[16]	13	10

-7-

7	11	15	19
10	14	18	3
13	17	2	6
16	1	5	9
0	[4]	8	12

-8-

16	17	18	19
12	13	14	15
8	9	10	11
4	5	6	7
0	[1]	2	3

-9-

4	9	14	19
3	8	13	18
2	7	12	17
1	6	11	16
0	[5]	10	15

-1-

5 RANGE GATES
4 SWEEPS PER CPI
20 REQUIRED MEMORY CELLS
INCREMENT IS MODULO-19

Figure 8 - Representative Addressing - Small Array

address of the first cell of the second sweep of each CPI is numerically equal to the address counter increment (modulo 19) for the next CPI. In the first CPI, the increment is 1 and information is stored in sequential locations for each gate of the first sweep followed by each gate of the second sweep, etc. The address for storing the first gate of the second sweep is 5 so that is the increment to be used for storing sweeps five through eight. Since the memory is of the read/modify/write type, the contents of cells 0-5-10-15 are read out as sweep five is being loaded in. Note that these cells contain the four samples of gate #1 taken in the first CPI. In this way, corner-turning is accomplished. Note also that the increment cycles through nine numbers and the tenth CPI is addressed exactly like the first CPI.

These same principles were used for the 7600-cell array in the MTD, with the increment cycling through 592 numbers before repeating. The address of the first gate of the second sweep is stored and held as the increment for the next CPI. If the address number is greater than 7599, the number is reduced by that amount before application to the memory.

The strobe RI which enters a new piece of data into memory also increments the address counter. The data-ready strobe ST from the memory is used to gate the signals out of memory to the rest of the MTD as far as the entrance into the weighting circuits. Details of memory operation may be found in the Standard Memories Inc. manual.

C. Single Range Gate Pickoff (For testing only)

The pulse from the selected range gate generator SRG in the timing section is used to gate the I & Q data from that particular gate into registers. The contents of the I register is then gated to output lines and a strobe sent

to the NOVA computer. Approximately 100 μsecs later the Q data is put on line and a second strobe sent. One bit is added to the words to identify the data. This bit is 1 in an I word and 0 in a Q word.

V. SATURATION DETECTOR AND INTERFERENCE ELIMINATOR

The interference eliminating circuits are shown in the block diagram of Figure 9. The magnitude of each of the 10 pulses is taken by adding the absolute values of I & Q. This algorithm is quite crude but still is accurate within 1 dB. The 10 magnitudes are summed and divided by two forming a number that is five times the average magnitude. The 10 magnitudes are also stored in a shift register delay line until the average has been computed. They are then compared sequentially with the five times average and if any one exceeds this number a flip-flop is set. This information is held until all Doppler processing has taken place and used to inhibit any threshold crossings that might occur in that range gate during the CPI interval.

The saturation detection circuits are shown in the block diagram of Figure 10. Saturation is defined as occurring whenever the four most significant bits of the I or Q signal are all ones or all zeros at the output of the core memory. The word is expressed in offset binary code so these conditions represent about 95% peak signal of either polarity. If saturation exists a flip-flop is set and held until the entire ten samples have been tested. This is necessary because if any I or Q sample saturates the A/D converters, all results from those 10 samples are void. The output of the flip-flop is stored for use in the threshold circuits at the appropriate time.

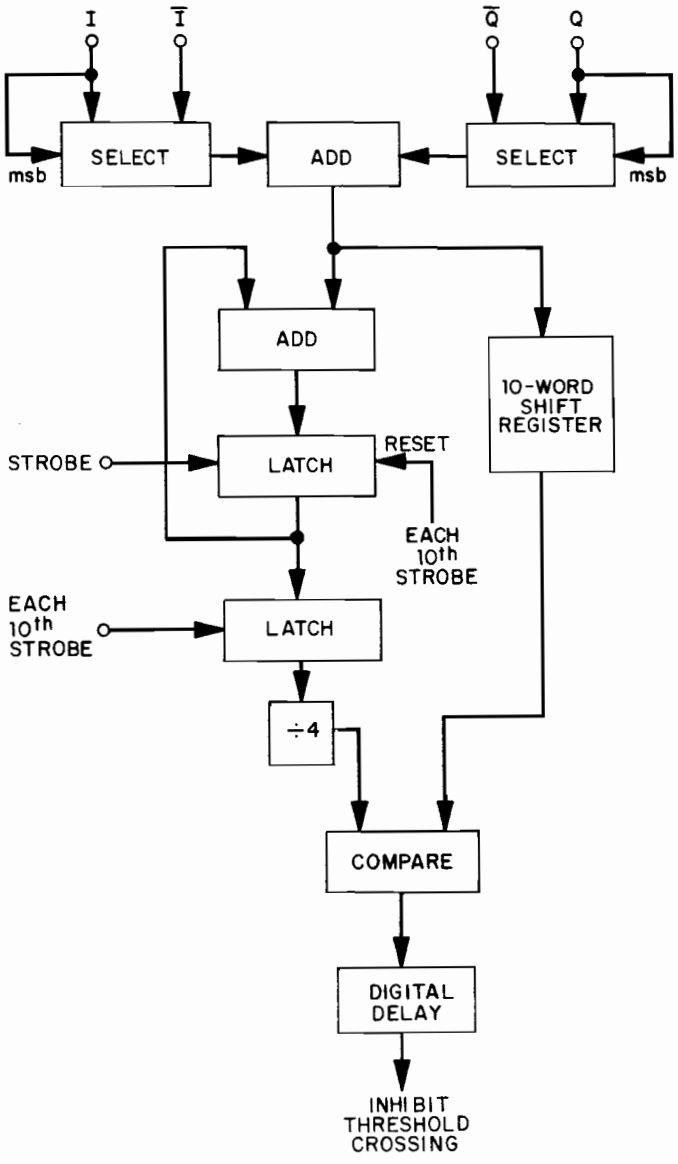


Figure 9 - Interference Eliminator Block Diagram

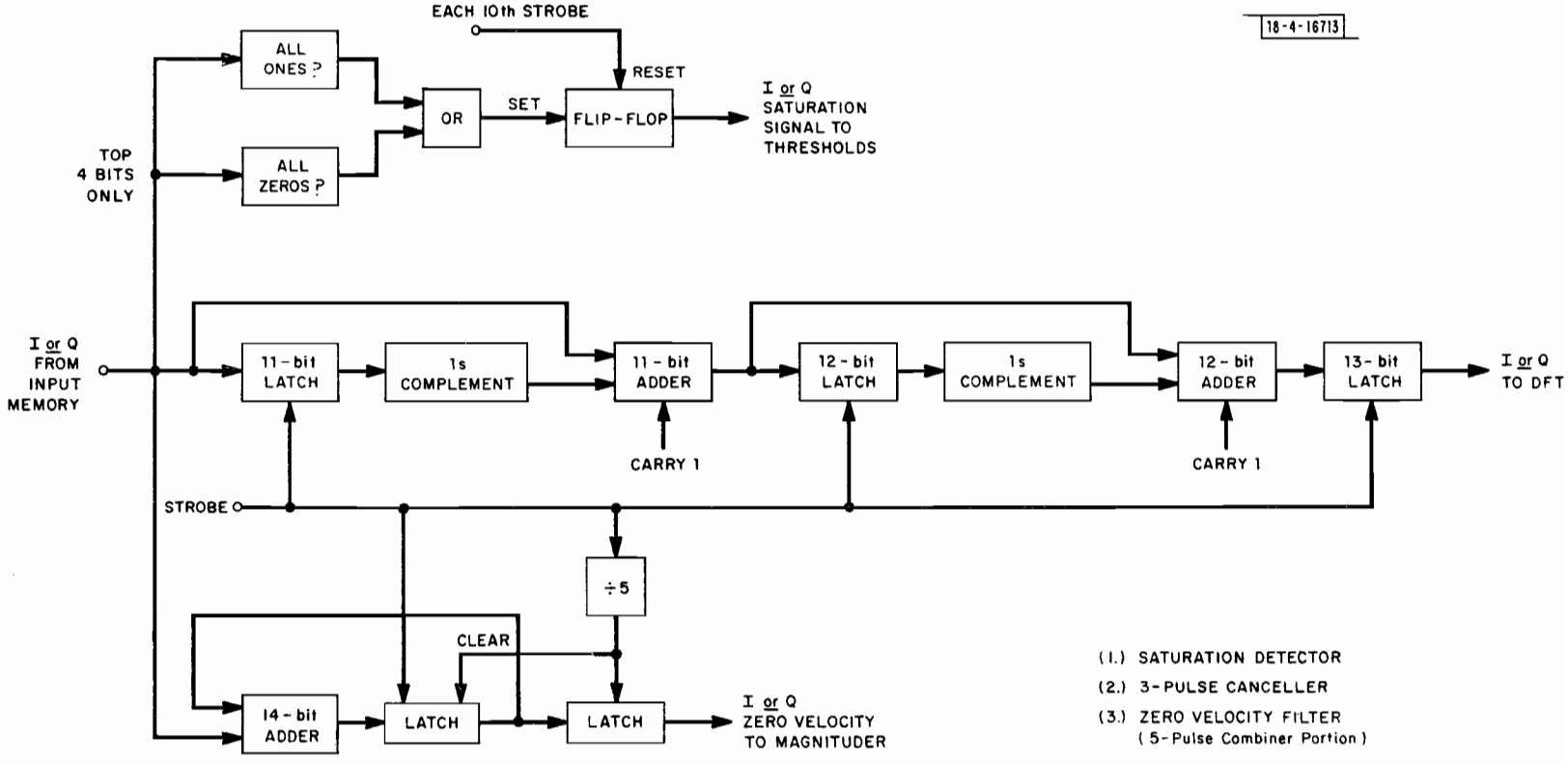


Figure 10 - Saturation Detector, 3-pulse Canceller, Zero Velocity Filter

VI. THREE-PULSE CANCELLER

The canceller is also shown in Figure 10. The circuits perform a subtraction function by taking the 1's complement of the subtrahend and adding to the minuend with a carry. The algorithm is A-2B+C, where A, B, C are successive input samples in I or Q. Passage through the canceller is time by the read strobes (ST) generated by the memory. Since complete passage requires three strobes, the output from the canceller after the first two strobes is meaningless and is ignored by succeeding circuits. At this point the 11-bit word from the memory has grown to a possible 13 bits for completely coherent signals.

VII. ZERO VELOCITY FILTER

The first part of the zero velocity filter (ZVF) is shown in Figure 10. The algorithm is to accumulate the I and Q signals in registers for the first five input signals and take the magnitude of the result. The process is repeated for the second five signals of the ten and the two magnitudes are then added to form a number indicating the strength of the zero velocity component of the signal. Passage through the accumulators is controlled by the read strobe (ST) generated in the core memory.

VIII. DISCRETE FOURIER TRANSFORMER AND CONTROLLER

This portion of the MTD consists of those subsystems shown in the block diagram of Figure 11. The DFT is really a small computer and the controller operates it with a hard-wired program of 80 instructions. The last eight of each ten I and Q signals from the canceller are stored in a scratch-pad integrated circuit memory. These are then read out and operated on by the complex combiner and $1/\sqrt{2}$ multiplier in various combinations with intermediate

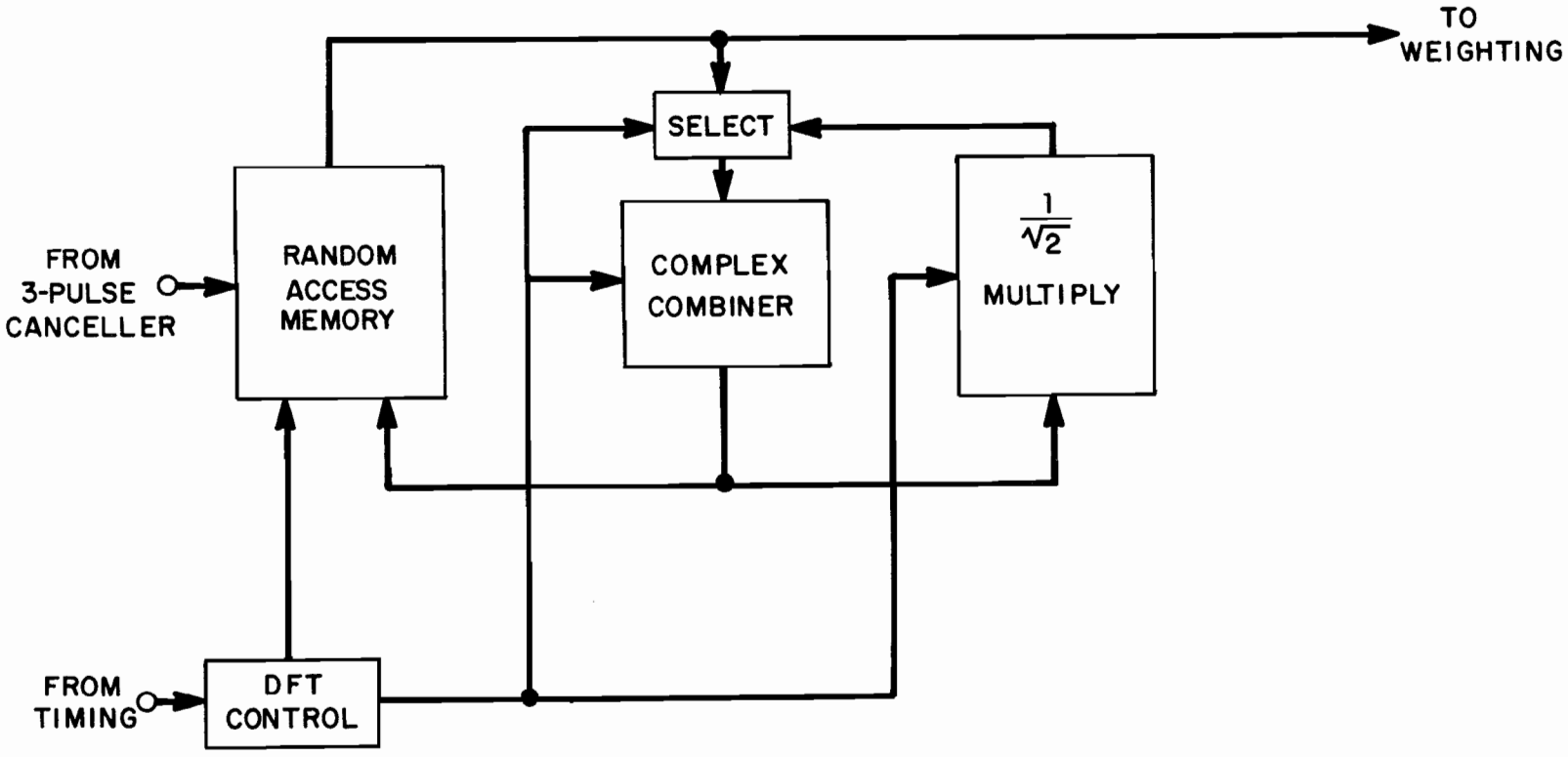


Figure 11 - Discrete Fourier Transform Gross Block Diagram

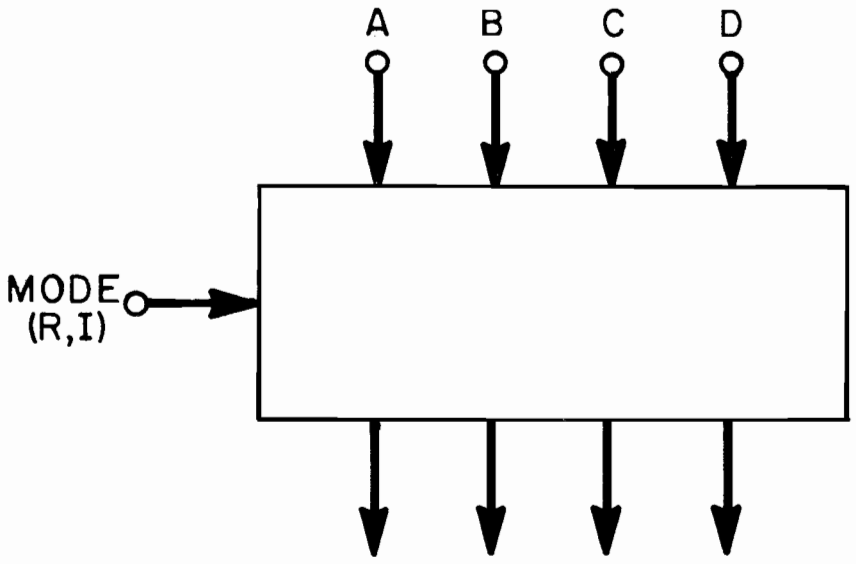
results being stored back in the IC memory. After all operations have been completed the transformed numbers are strobed out to a circuit which properly weights them.

The I and Q components of each number can be though of as the real and imaginary parts of a complex number for purposes of this discussion, and each such complex number therefore has 32 bits. Scratch-pad storage for 14 of these 32-bit words is required for complete operation of the DFT. Eight random-access memory chips are used, each with 16, 4-bit words.

Figure 12 is a functional diagram of the complex combiner. There are four 16-bit inputs, four 16-bit outputs and a mode switching line. In each of the two modes the four inputs are combined to form the sums and differences as indicated in Figure 12a. If we let $\dot{X}$ be A+jB and $\dot{Y}$ be C+jD, then the results of complex combining are as shown in Figure 12b.

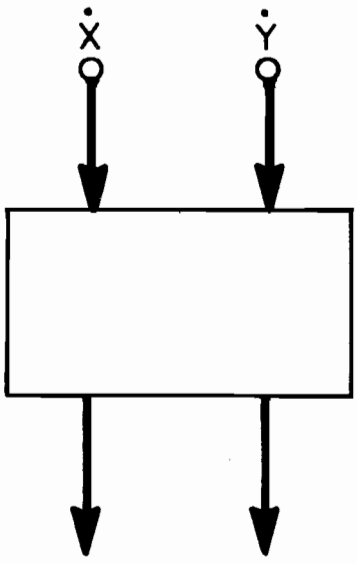
Figure 13 is a flow diagram for an 8-point DFT. Each square represents one pass through the complex combiner, with or without the $1/\sqrt{2}$ multiplier as the case may be. Three distinct time periods exist in the DFT, represented by the three columns of squares. Note that each column uses all the inputs available to that column and that after each column the input information for the column is no longer needed. It is this last property that makes the amount of scratch-pad storage manageable.

There are four different types of pass. A type 1 pass is formed by using the complex combiner in mode R and a type 2 by using it in mode I. A type



MODE				
R	A+C	B+D	A−C	B−D
I	A−D	B+C	A+D	B−C

(a)



MODE		
R	Ẋ+Ẏ	Ẋ−Ẏ
I	Ẋ+jẎ	Ẋ−jẎ

(b)

Figure 12 - Discrete Fourier Transform Functional Block Diagram

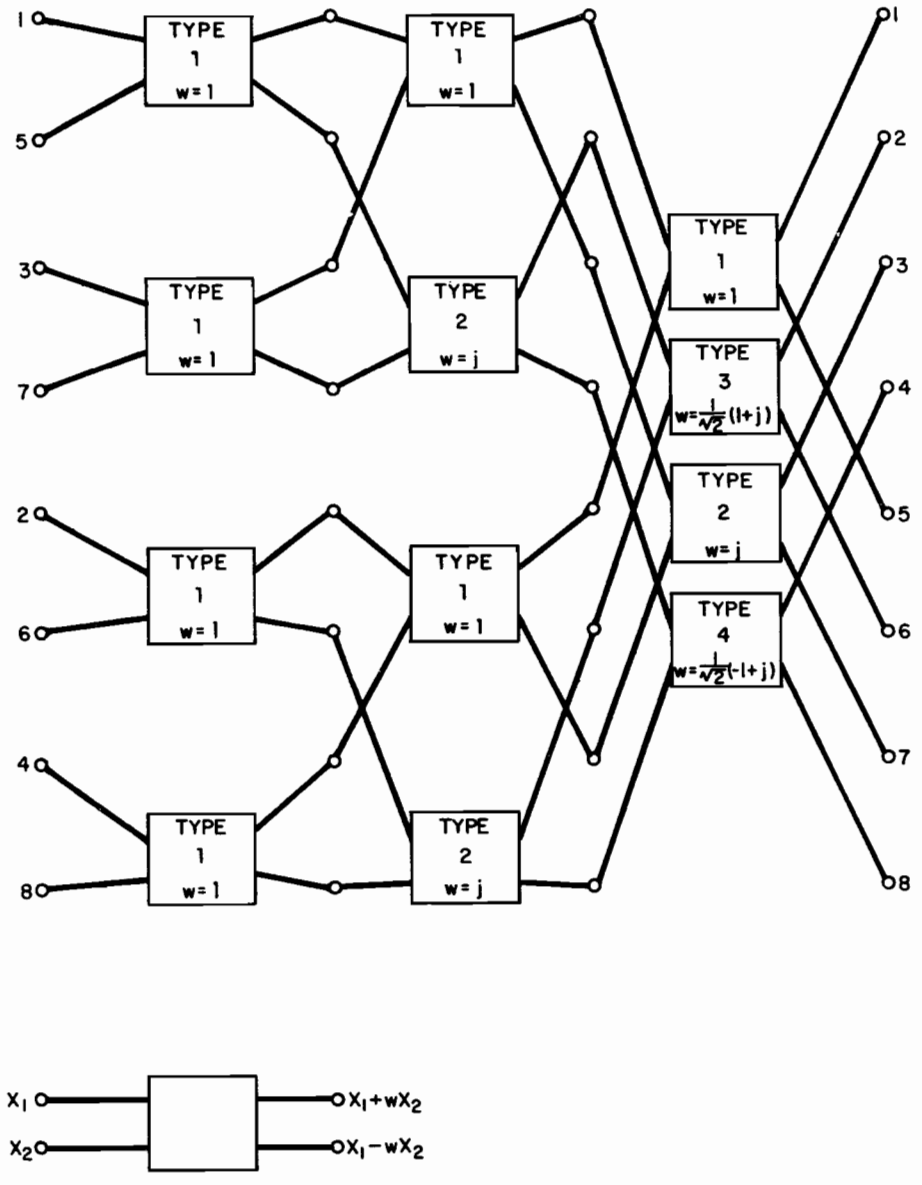


Figure 13 - Discrete Fourier Transform Flow Diagram

3 pass is formed by using mode R and the multiplier, while a type 4 uses mode I and the multiplier. Table 2 shows the complex mathematics for each type of pass. Note that for types 3 and 4 the quantities in brackets are the sum and difference of the parts of $\dot{X}_2$. These are formed by putting $\dot{X}_2$ into both sides of the combiner, placing it in the I mode and taking the result from the left half of the combiner output as shown in Figure 12a. This complex number is then multiplied by $1/\sqrt{2}$ and run through the combiner again in conjunction with $\dot{X}_1$ to form the complete pass.

Figure 14 is a detailed block diagram of the DFT hardware. A pass through the combiner is performed by loading the complex number $\dot{X}_1$ from scratch memory into a 32-bit register with strobe LOAD1. Then $\dot{X}_2$ is loaded through selectors into a register with strobe LOAD2. This strobe also clocks $\dot{X}_1$ along into its second input register. The two words, at this point, are presented to the various adders, negators and selectors that form the combiner proper. A few hundred nsecs later the desired sums and differences appear at the output and are strobed back into memory. If a multiply is to take place, the left half of the output information is clocked into a register by $\underline{\sqrt{2}\text{LOCK}}$ pulse. The multiplication by $1/\sqrt{2}$ is carried out by forming the sum of $(1/2 + 1/8 + 1/16 + 1/64 + 1/256)$ which equals 0.707031, a reasonable approximation to the desired factor. Since there is time to spare, the real and imaginary parts are multiplied one after the other and the products stored. The input selectors at the top of the combiner are then switched by the $\underline{\sqrt{2}\text{TRANSFER}}$ signal and the new product $1/\sqrt{2}\ [R(\dot{X}_2) \pm I(\dot{X}_2)]$ is strobed into

TABLE 2

DFT PASS EQUATIONS

W has 4 values

$$W_o = 1$$

$$W_1 = j$$

$$W_2 = 1/\sqrt{2}\,(1 + j)$$

$$W_3 = 1/\sqrt{2}\,(-1 + j)$$

Type 1

$$R(Y_1) = R(X_1) + R(X_2)$$

$$I(Y_1) = I(X_1) + I(X_2)$$

$$R(Y_2) = R(X_1) - R(X_2)$$

$$I(Y_2) = I(X_1) - I(X_2)$$

Type 2

$$R(Y_1) = R(X_1) - I(X_2)$$

$$I(Y_1) = I(X_1) + R(X_2)$$

$$R(Y_2) = R(X_1) + I(X_2)$$

$$I(Y_2) = I(X_1) - R(X_2)$$

Type 3

$$R(Y_1) = R(X_1) + 1/\sqrt{2}\,[R(X_2) - I(X_2)]$$

$$I(Y_1) = I(X_1) + 1/\sqrt{2}\,[R(X_2) + I(X_2)]$$

$$R(Y_2) = R(X_1) - 1/\sqrt{2}\,[R(X_2) - I(X_2)]$$

$$I(Y_2) = I(X_1) - 1/\sqrt{2}\,[R(X_2) + I(X_2)]$$

Type 4

$$R(Y_1) = R(X_1) - 1/\sqrt{2}\,[R(X_2) + I(X_2)]$$

$$I(Y_1) = I(X_1) + 1/\sqrt{2}\,[R(X_2) - I(X_2)]$$

$$R(Y_2) = R(X_1) + 1/\sqrt{2}\,[R(X_2) + I(X_2)]$$

$$I(Y_2) = I(X_1) - 1/\sqrt{2}\,[R(X_2) - I(X_2)]$$

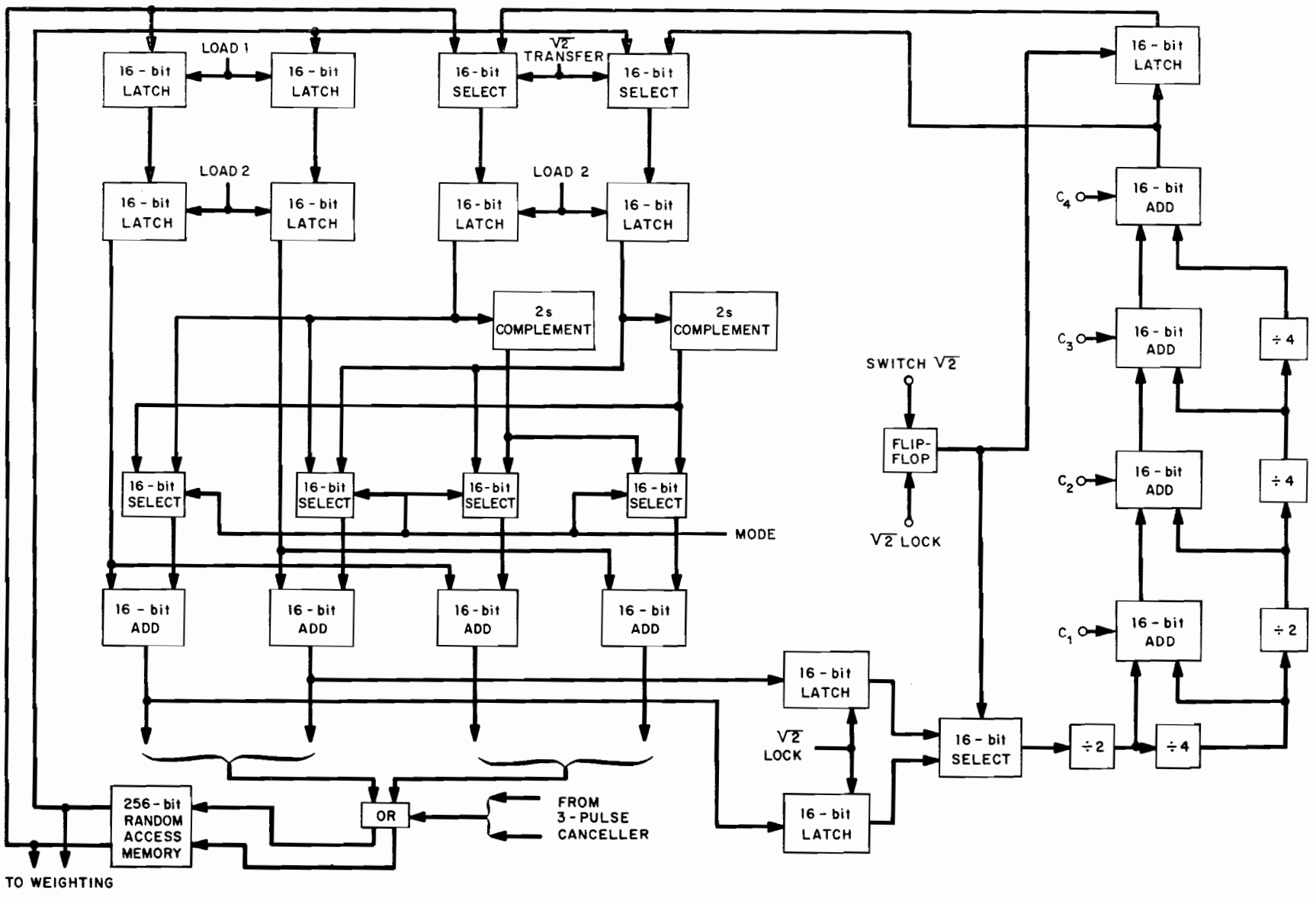


Figure 14 - Complex Combiner and Multiplier Block Diagram

the input register by LOAD2. The pass is then completed by loading $\dot{X}_1$ in the left side register and continuing in the usual way.

A shift-right operation results in truncation which makes the result always more negative than actual division would produce. Since the multiplier uses five such shifts along with addition, the error can be substantial. For example, the multiplication by $1/\sqrt{2}$ of +1 and -1 yields 0 and -5 respectively. By using the carry inputs of the four adders and some logic, the error can be greatly reduced and made equal for positive and negative numbers. The algorithm used for adding corrections with the carry bits is:

If input number is positive and divisible by 8, add 0.
If input number is positive and not divisible by 8, add 1.
If input number is negative and even, add 3.
If input number is negative and odd, add 4.

Table 3 gives the results for multiplying small numbers with this algorithm. As the numbers get larger, the approximation is closer to $1/\sqrt{2}$.

The DFT controller shown in Figure 15 is a stored program which cycles through 80 instructions in 7.75 μsecs. Each instruction has an operand portion and a scratch-pad memory address portion. The operand portion causes one or more of 12 possible timing pulses to be generated and the address specifies which memory cell is to be affected. Table 4 is a list of the 12 possible pulses along with their uses. Table 5 lists the stored program, while Table 6 traces the full three passes of one range gate through the DFT. Note that since three passes are required for each gate, there are three gates being processed at all times with operations being inter-leaved. Table 7 shows the three passes inter-leaved.

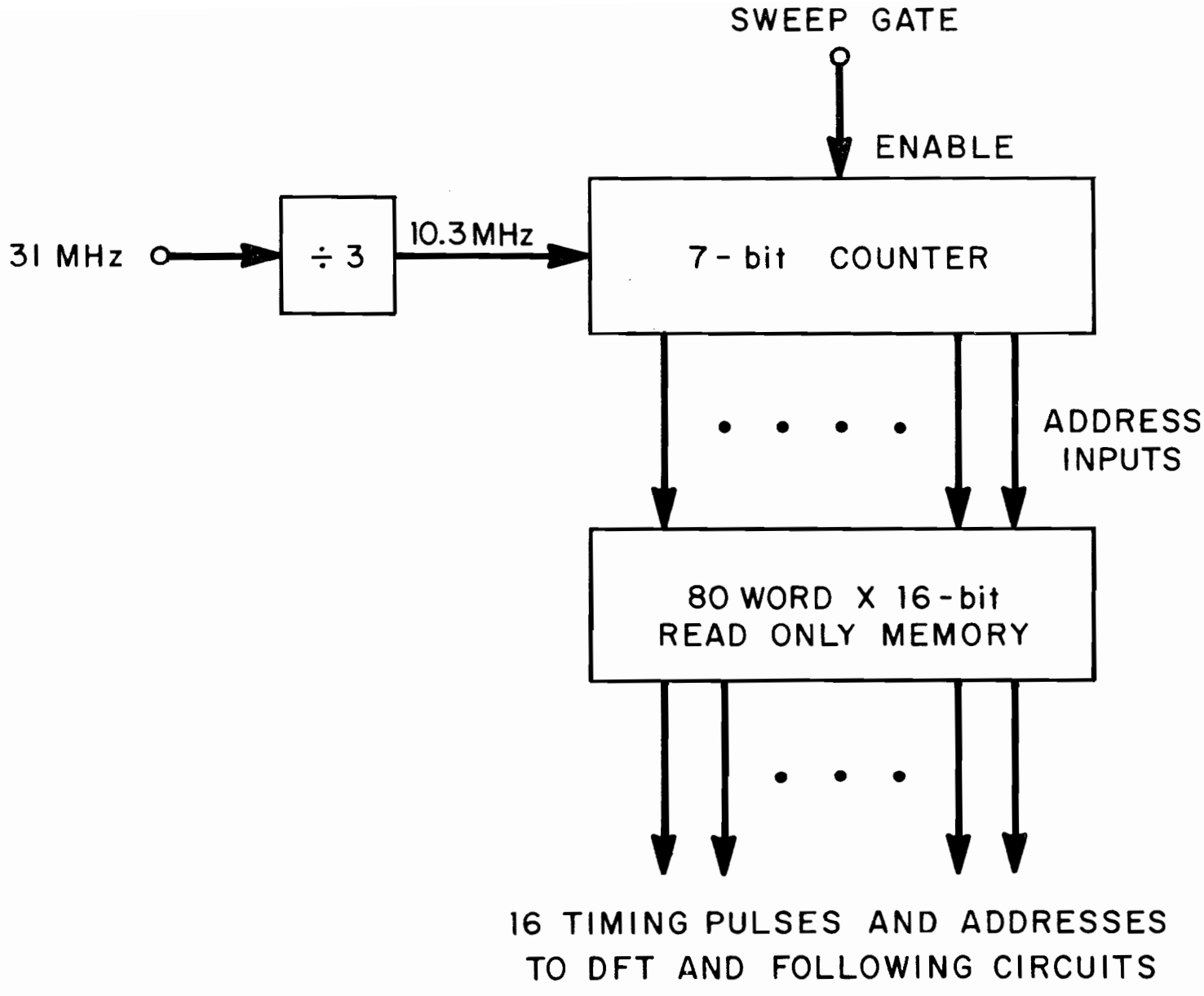


Figure 15 - Discrete Fourier Transform Controller Block Diagram

TABLE 3

APPROXIMATION OF $\frac{1}{\sqrt{2}}$

N	$1/\sqrt{2}$ (+N)	$1/\sqrt{2}$ (-N)	Value of $1/\sqrt{2}$	N	$1/\sqrt{2}$ (+N)	$1/\sqrt{2}$ (-N)	Value of $1/\sqrt{2}$
0	0	--	--	28	19	-19	.679
1	1	-1	1.000	29	19	-19	.655
2	2	-2	1.000	30	20	-20	.667
3	2	-2	.667	31	20	-20	.645
4	3	-3	.750	32	22	-21	.688/.656
5	3	-3	.600	33	23	-23	.697
6	4	-4	.667	34	24	-24	.706
7	4	-4	.571	35	24	-24	.686
8	5	-5	.625	36	25	-25	.694
9	6	-6	.667	37	25	-25	.676
10	7	-7	.700	38	26	-26	.684
11	7	-7	.636	39	26	-26	.667
12	8	-8	.667	40	27	-27	.675
13	8	-8	.615	41	28	-28	.683
14	9	-9	.643	42	29	-29	.690
15	9	-9	.600	43	29	-29	.674
16	11	-10	.688/.625	44	30	-30	.682
17	12	-12	.706	45	30	-30	.667
18	13	-13	.722	46	31	-31	.674
19	13	-13	.684	47	31	-31	.660
20	14	-14	.700	48	33	-32	.688/.667
21	14	-14	.667	49	34	-34	.694
22	15	-15	.682	50	35	-35	.700
23	15	-15	.652	51	35	-35	.686
24	16	-16	.667	52	36	-36	.692
25	17	-17	.680	53	36	-36	.679
26	18	-18	.692	54	37	-37	.685
27	18	-18	.667	55	37	-37	.673

TABLE 4

DFT PROGRAM SIGNAL DEFINITIONS

MS	-	Strobes signals from the weighting circuits to the magnitude-taking circuits.
OS	-	Strobes signals from the DFT scratch-pad memory to the weighting circuits.
LOAD	-	Strobes signals from the DFT scratch-pad memory into the left side of the complex combiner.
L&G	-	Strobes signals from the DFT scratch-pad memory into the right side of the complex combiner.
SI	-	Strobes signals from the 3-pulse canceller into the DFT scratch-pad memory.
SS	-	Strobes results from the left side of the complex combiner into the DFT scratch-pad memory.
S	-	Strobes results from the right side of the complex combiner into the DFT scratch-pad memory.
TFR	-	Switches the input selectors on the complex combiner to receive multiplier outputs.
R/I	-	Changes the complex combiner from "R" to "I" mode.
LO	-	Latches the left side outputs from the combiner into the multiplier input registers.
LOS	-	Latches the output of the first half multiplication into storage and selects the second half of the multiplier input.
ZS	-	Strobes the output of the zero velocity filter accumulators into the magnitude-taking circuits.

TABLE 5

DFT HARD-WIRED PROGRAM

	MS OS SS S	SI Load TFR R/I	L&G LOS LO ZS	Mem. Add.
0			1	0110
1	1			0000
2	1			1100
3	1			0010
4	1			0110
5		1		0001
6			1	0011
7				0000
8		1		0100
9	1 1			0011
A	1			1010
B			1	1000
C	1			1011
D				0000
E	1			0100
F	1			1000
10		1		0010
1	1		1	0100
2	1			1101
3		1		0001
4	1			1001
5	1			0100
6		1		0110
7		1	1	1000
8	1	1		0000
9	1			1110

TABLE 5 (cont.)

	MS OS SS S	SI Load TFR R/I	L&G LOS LO ZS	Mem. Add.
A	1			0110
B	1			1000
C		1		0110
D		1	1	0110
E				0000
F				0000
20	1	1	1	0011
1			1	1001
2			1	0000
3		1		0011
4	1			1110
5	1		1	1001
6		1		1010
7	1	1	1	0100
8	1			1110
9				0000
A	1			1010
B		1		0101
C	1	1		1011
D		1	1	0100
E			1	0000
F		1		1000
30	1			0101
1	1			1100
2	1	1	1	1000
3				0101

TABLE 5 (cont.)

	MS OS SS S	SI Load TFR R/I	L&G LOS LO ZS	Mem. Add.
4		1		0101
5		1	1	0001
6			1	0101
7				0000
8				0000
9	1			0001
A	1		1	0101
B		1		0110
C	1			1010
D		1		0111
E				0000
F		1	1	0000
40		1		0011
1				0111
2	1			1000
3	1 1	1		1101
4			1	0111
5	1			1000
6				0000
7	1			0011
8	1			0111
9		1		0101
A	1	1	1	0111
B	1			1001
C		1		1000
D	1			0101
E	1			0111
F		1		0000

TABLE 6

PASSAGE OF ONE RANGE GATE THROUGH THE DFT PROGRAM

Hexadecimal Instruction #	Function
13	Input sample #1 from canceller.
1C	Input sample #2 from canceller.
23	Input sample #3 from canceller.
2D	Input sample #4 from canceller.
2E	Transfer 1st half ZVF accumulation to magnituder.
34	Input sample #5 from canceller.
35	Load sample #1 into left side combiner.
36	Load sample #5 into right side combiner, perform type 1 pass.
39	Store left side combiner in storage #1.
3A	Store right side combiner in storage #5.
3B	Input sample #6 from canceller.
40	Load sample #3 into left side combiner.
43	Input sample #7 from canceller.
45	Load sample #7 into right side combiner, perform type 1 pass.
47	Load storage #5 into left side combiner.
48	Store left side combiner into storage #3.
49	Store right side combiner into storage #7.
4A	Load storage #7 into right side combiner, perform type 2 pass.
4C	Input sample #8 from canceller.
4D	Store left side combiner into storage #5.
4E	Store right side combiner into storage #7.
4F	Load sample #2 into left side combiner.
0	Load sample #6 into right side combiner, perform type 1 pass.
3	Store left side combiner into storage #2.
4	Store right side combiner into storage #6.

TABLE 6 (cont.)

5	Load storage #1 into left side combiner.
6	Load storage #3 into right side combiner, perform type 1 pass.
8	Load sample #4 into left side combiner.
9	Store left side combiner into storage #1.
A	Store right side combiner into storage #3.
B	Load sample #8 into right side combiner, perform type 1 pass.
E	Store left side combiner into storage #4.
F	Store right side combiner into storage #8.
10	Load storage #2 into left side combiner.
11	Load storage #4 into right side combiner, perform type 1 pass.
14	Store left side combiner into storage #2.
15	Store right side combiner into storage #4.
16	Load storage #6 into left side combiner.
17	Load storage #8 into right side combiner, perform type 2 pass.
1A	Store left side combiner into storage #6.
1B	Store right side combiner into storage #8.
1D	Load storage #6 into left side combiner.
1E	Load storage #6 into right side combiner, perform type 2 pass.
21	Load storage #1 into left side combiner, lock combiner output into multiplier register.
22	Load storage #2 into right side combiner, perform type 1 pass.
24	Load storage #3 into left side combiner.
25	Store left side combiner into storage #1, lock multiplier output and switch input.
26	Store right side combiner into storage #2.
27	Load storage #4 into right side combiner, perform type 2 pass.
28	Output storage #1 to weighting circuits.

TABLE 6 (cont.)

2A	Store left side combiner into storage #3.
2B	Load storage #5 into left side combiner.
2C	Store right side combiner into storage #4, transfer multiplier to right side combiner.
2D	Perform type 1 pass. (Really type 3).
2F	Load storage #8 into left side combiner.
30	Store left side combiner into storage #5.
31	Store right side combiner into storage #6.
32	Load storage #8 into right side combiner, perform type 2 pass.
33	Output storage #5 to weighting circuits.
35	Lock combiner output into multiplier register.
3A	Lock multiplier output and switch input
3C	Output storage #3 to weighting circuits.
3D	Load storage #7 into left side combiner.
3E	Transfer multiplier output to right side combiner.
3F	Perform type 2 pass. (Really type 4)
42	Store left side combiner into storage #7.
43	Transfer data out of magnituder. (Filter #1)
44	Store right side combiner into storage #8.
46	Output storage #7 to weighting circuits.
4A	Transfer data out of magnituder. (Filter #2)
4B	Output storage #2 to weighting circuits.
1	Transfer data out of magnituder. (Filter #3)
2	Output storage #6 to weighting circuits.
9	Transfer data out of magnituder. (Filter #4)
C	Output storage #4 to weighting circuits.
11	Transfer data out of magnituder. (Filter #5).
12	Output storage #8 to weighting circuits.
18	Transfer data out of magnituder (Filter #6)
19	Output storage #1 to weighting circuits
1B	Transfer 2nd half ZVF accumulation to magnituder.
20	Transfer data out of magnituder. (Filter #0)
27	Transfer data out of magnituder. (Filter #7)

TABLE 7

INTERLEAVING OF THREE PASSES THROUGH THE DFT PROGRAM

small letters = pass 1
LARGE LETTERS = pass 2
Script letters = pass 3

0	#6 INTO RT. SIDE; TYPE 1 PASS.
1	*Mag. output filter #3*
2	*#6 to weighting*
3	LEFT SIDE INTO #2.
4	RT. SIDE INTO #6.
5	#1 INTO LEFT SIDE.
6	#3 INTO RT. SIDE; TYPE 1 PASS.
8	#4 INTO LEFT SIDE.
9	LEFT SIDE INTO #1; *mag. output filter #4*
A	RT. SIDE INTO #3.
B	#8 INTO RT. SIDE; TYPE 1 PASS.
C	*#4 to weighting*
E	LEFT SIDE INTO #4.
F	RT. SIDE INTO #8.
10	#2 INTO LEFT SIDE.
11	#4 INTO RT. SIDE; TYPE 1 PASS; *mag. output filter #5*
12	*#8 to weighting*
13	input sample #1.
14	LEFT SIDE INTO #2.
15	RT. SIDE INTO #4.
16	#6 INTO LEFT SIDE.
17	#8 INTO RT. SIDE; TYPE 2 PASS.
18	*Mag. output filter #6*
19	*#1 to weighting*
1A	LEFT SIDE INTO #6.
1B	RT. SIDE INTO #8; *2nd half zvf to magnituder*
1C	input sample #2.
1D	#6 INTO LEFT SIDE.
1E	#6 INTO RT. SIDE; TYPE 2 PASS.
20	*Mag. output filter #0*
21	#1 INTO LEFT SIDE; LOCK MPR INPUT.
22	#2 INTO RT. SIDE; TYPE 1 PASS.
23	input sample #3.
24	#3 INTO LEFT SIDE.
25	LEFT SIDE INTO #1; LOCK & SWITCH MPR.
26	RT. SIDE INTO #2.
27	#4 INTO RT. SIDE; TYPE 2 PASS; *mag. output filter #7*
28	#1 TO WEIGHTING.
2A	LEFT SIDE INTO #3.
2B	#5 INTO LEFT SIDE
2C	RT. SIDE INTO #4; MPR TO RT. SIDE.
2D	TYPE 3 PASS; input sample #4.
2E	1st half zvf to magnituder.

TABLE 7 (cont.)

2F	#8 INTO LEFT SIDE
30	LEFT SIDE INTO #5.
31	RT. SIDE INTO #6.
32	#8 INTO RT. SIDE; TYPE 2 PASS.
33	#5 TO WEIGHTING.
34	input sample #5.
35	LOCK MPR INPUT; #1 into left side.
36	#5 into rt. side; type 1 pass.
39	left side into #1.
3A	LOCK & SWITCH MPR; rt. side into #5.
3B	input sample #6.
3C	#3 TO WEIGHTING.
3D	#7 INTO LEFT SIDE.
3E	MPR TO RT. SIDE.
3F	TYPE 4 PASS.
40	#3 into left side.
43	MAG. OUTPUT FILTER #1; input sample #7.
44	LEFT SIDE INTO #8.
45	#7 into rt. side; type 1 pass
46	#7 TO WEIGHTING.
47	#5 into left side.
48	left side into #3.
49	rt. side into #7.
4A	MAG. OUTPUT FILTER #2; #7 into rt. side; type 2 pass.
4B	#2 TO WEIGHTING.
4C	input sample #8.
4D	left side into #5.
4E	rt. side into #7.
4F	#2 into left side.

The program is stored in a read-only memory (ROM) which is cycled through its 80 addresses by a counter running from a 10.3 MHz clock. The clock is formed by dividing the 31 MHz signal by three. The counter is reset to zero just before the first signal for each range gate is output from the core memory, and is only allowed to count during the times that data is actually coming from memory.

The saturation detector, canceller, ZVF and DFT circuitry are located on the lower and inside upper panels in the front of drawer "D". Small extra subpanels have been added to these to hold D/A converter modules used in testing and monitoring. The interference eliminator is located on the outside upper panel in front of drawer "D".

IX. WEIGHTING CIRCUITS

The weighting circuits shown in Figure 16 accept nine successive signals in both I and Q from the DFT for each range gate. These represent filter outputs zero through seven, with zero repeated at the end. The weighting algorithm is such that each value of I or Q is diminished by 1/4 of the two adjacent filter values. The reason the zeroth filter appears twice is that 1/4 of its value must be subtracted from both the first and the seventh filter values. Implementation is by the "pipeline" technique such that the weighted output is $B - (1/4A + 1/4C)$, where A, B, C represent successive filter outputs. The first two numbers to issue from the weighting circuits are meaningless because three inputs are required to form the first valid output.

In Figure 16, one would expect carry B to be a one. This would normally be the case because carry B combines with the taking of the ones complement to perform the subtraction function. However, pursuing

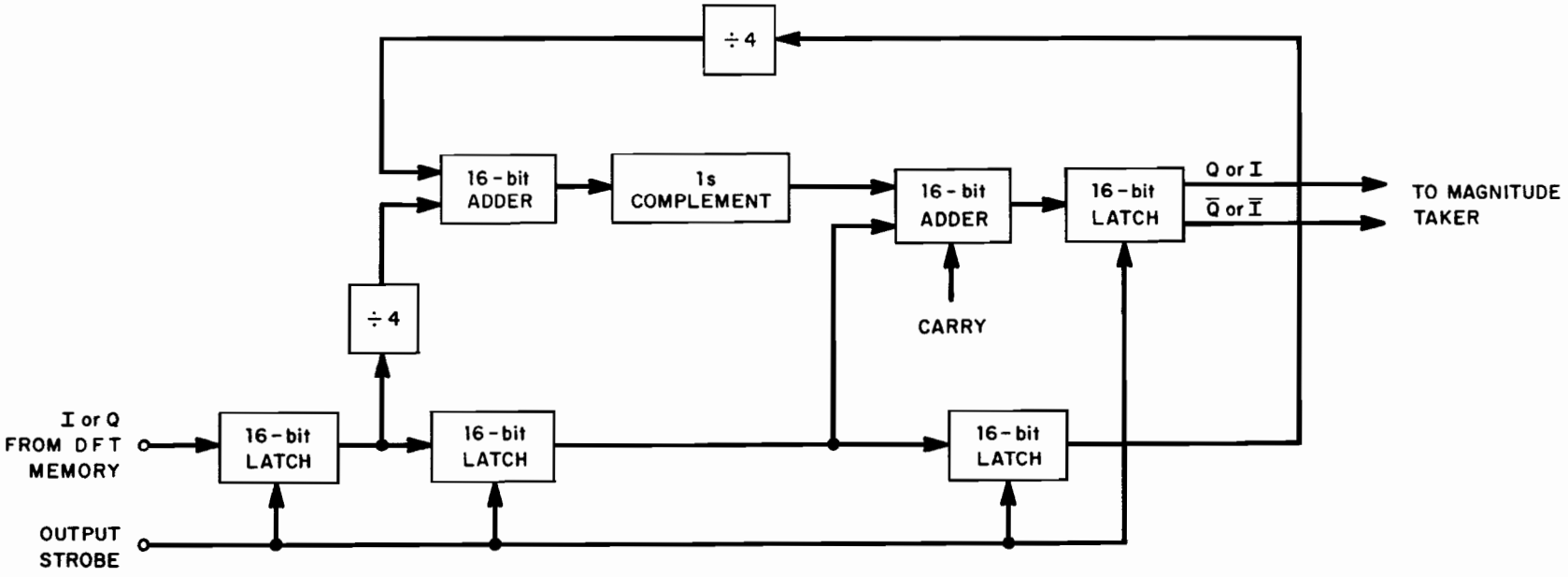


Figure 16 - Weighting Circuits Block Diagram

the same logic about truncation as in the $1/\sqrt{2}$ multiplier, shifting right two places makes both numbers too negative. On the average, the sum of the two fractions will be too negative by one, which is cancelled out by the action of taking the 1's complement. By eliminating the carry in the subtraction function (carry B) the truncation becomes a roundoff.

This weighting algorithm is the equivalent of a Hanning weighting function performed in the time domain. Figure 17 shows the responses of the weighted filters.

X. MAGNITUDE-CALCULATION CIRCUITS

The magnituder is shown in the block diagram of Figure 18. At the input is a select 1-of-2 circuit because the zeroth filter output from the DFT and weighting circuits must be replaced by the two accumulations of five samples from the ZVF. The operation of this selector is controlled by the ZS strobes from the DFT controller. From the selectors, I & Q pass through circuits which form their absolute values. Either the input value or its 1's complement is transmitted depending on the sign bit of the word. A pair of selectors and a comparitor form a circuit that determines the larger of I & Q and steers it to the LARGER output. Likewise, the lesser value is steered to the SMALLER output. One-eighth of LARGER is subtracted from LARGER leaving 7/8 and this is added to 1/2 SMALLER forming a new quantity. This new quantity is compared to LARGER and the greater value transmitted to the output circuits.

For all non-ZVF outputs the signals then pass through an adder which adds zero to the signal and is therefore transparent, and then through a selector to the thresholding equipment. When the first ZVF sum comes through the

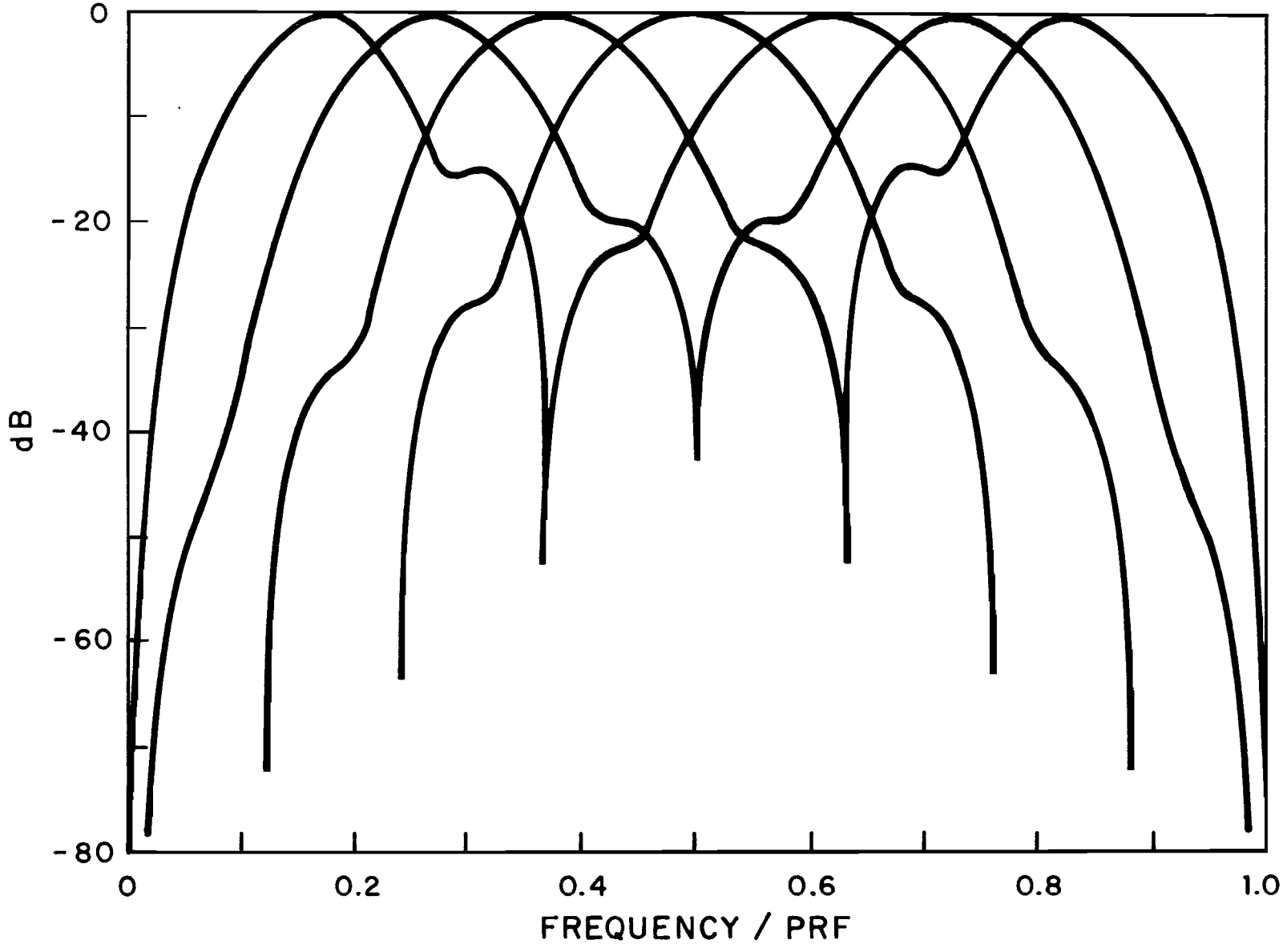


Figure 17 - Frequency Response of Weighted Filters

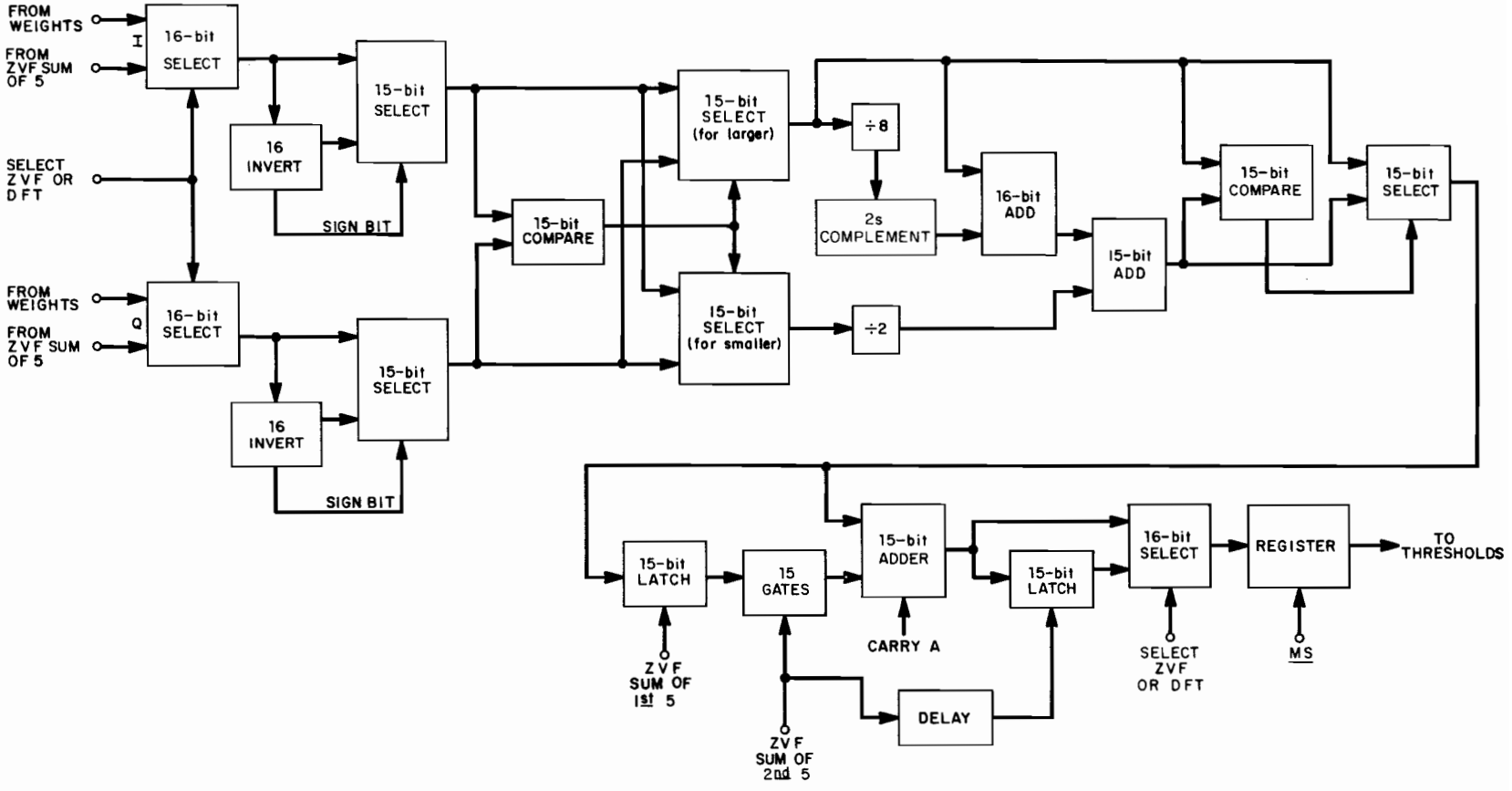


Figure 18 - Magnitude Forming Circuits Block Diagram

magnituder it is stored in a register. When the second sum appears at the adder input, the first sum is gated to the other side of the adder and the total sum is stored in a register at the adder output. Since it is desirable to have the eight filters presented to the thresholds in numerical order, the selector switches to this register to pick up the ZVF value during the time between transmission of the seventh and first filters. These eight filter values are strobed sequentially into a buffer register by the magnitude strobe (MS) pulse from the DFT controller.

This magnituding algorithm varies from the ideal value of $\sqrt{I^2 + Q^2}$ by less than 0.2 dB in the worst case. The maximum filter output magnitudes normalized to the center filter are as follows:

ZVF	.3125	-5.05 dB
Filter #1	.2288	-6.41 dB
Filter #2	.5557	-2.55 dB
Filter #3	.8707	-0.60 dB
Filter #4	1.0000	0 dB
Filter #5	.8707	-0.60 dB
Filter #6	.5557	-2.55 dB
Filter #7	.2288	-6.41 dB

This variation in gain is caused by the 3-pulse canceller function.

The weighting and magnituding equipment is located in the lower front panel of drawer "D".

XI. WEATHER THRESHOLD GENERATOR

This generator is shown in the block diagram of Figure 19 and can be thought of in four sections:

1. Running summer
2. Subtracter
3. Multiplier
4. Video generator

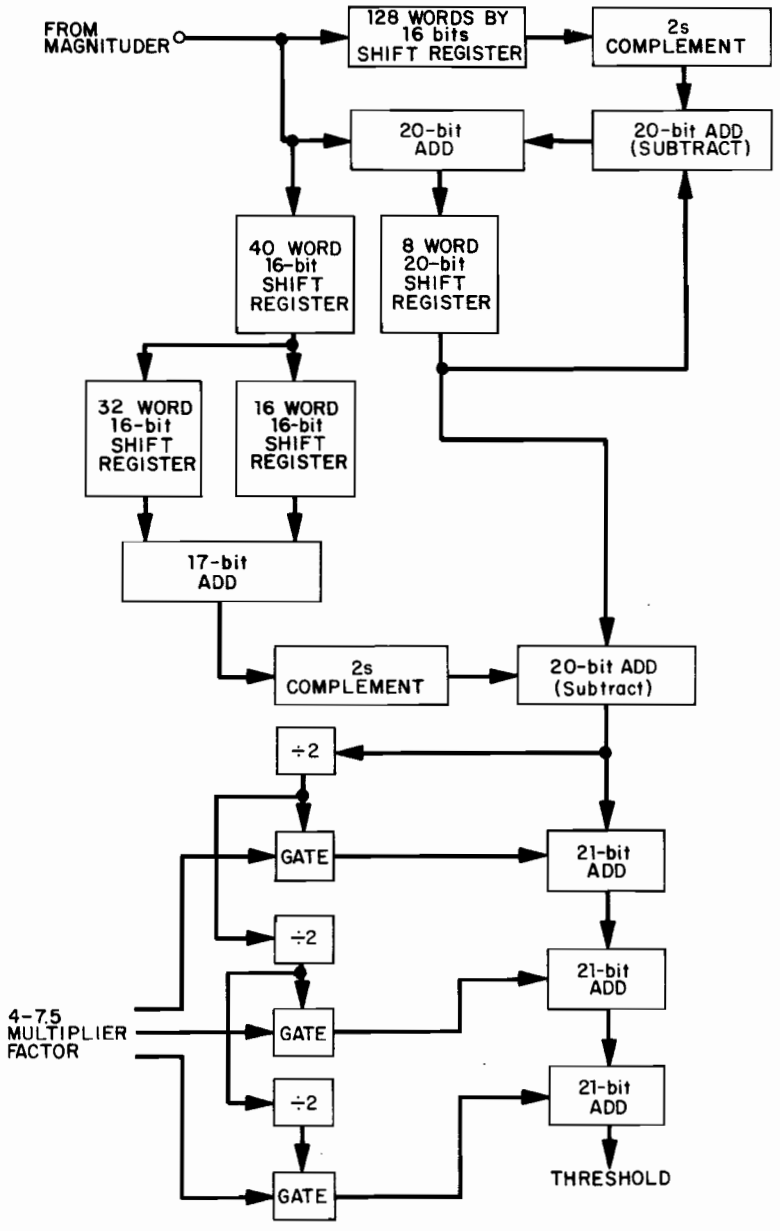


Figure 19 - Weather Threshold Generator Block Diagram

A. Running Summer

The purpose of the summer is to continuously compute the sum of the most recent 16 range gates on a filter-by-filter basis. This is accomplished by feeding the eight filter outputs sequentially into a delay line shift register range gate by range gate. The delay line is 128 words by 16 bits in size since 128 words are required for 16 gates of eight filters. A smaller 8-word by 20-bit shift register delay line holds the running sum for each filter. As each filter sum emits from this register it is used to generate a threshold. At the same time a new sum is generated by adding the value of the filter just coming from the magnituder and subtracting the value of the filter at the end of the 128-word delay line. This new sum is then stuffed back into the 8-word shift register and appears at its output exactly one gate (eight filters) later for use as the new threshold. This amounts to adding the newest value and subtracting the oldest value over 16 range gates on a continuing basis.

B. Subtracter

The signal that is going to be compared to this threshold is that which appears in the ninth gate of the 16. If this "target" happens to split two gates equally, the use of such a threshold requires a much larger S/N ratio than one would expect for detection. The effect of such range-splitting is minimized by not including the two gates adjacent to the target in the sum. The eighth and 10th gate outputs are added together and then subtracted from the sum of 16, thus making it a sum of 14. In order to prevent truncation, all arithmetic in the subtracter section contains 20-bit words.

C. Multiplier

The sum of 14 gate signals must be multiplied by a factor before application to the threshold crossing comparitor. This multiplier has seven

possible values ranging from 1/4 to 15/32 and is performed in two steps. First, the sum is multiplied by a factor ranging from 1 to 1 7/8. This is accomplished by taking the number and adding one or more of the fractions 1/2, 1/4, 1/8 of its value or none of them. The second step is a division by four accomplished by shifting right two places. The final threshold then is a number ranging from 3.50 to 6.56 times the average of the signals in the 14 gates and is adjustable in eight steps. The selection of this multiplier factor for filters 2 through 6 is made by inserting a patch plug onto socket #X-J2 on the lower rear panel of drawer "D".

Filters 1 and 7 normally have much smaller numbers at the canceller output than the rest of the filters because of the shape of the canceller function. As a result of this, quantization noise is a problem in computing the threshold for these two filters. It was found that if all filter thresholds had the same multiplier factor, there were excessive false alarms in filters 1 and 7. Consequently, the multiplier factor for those two filters has been made independent of filters 2 through 6 and is set by inserting a patch onto socket #J-J2.

The shift registers in the threshold generator are clocked by THRESHSTROBE, a signal made by combining the magnitude strobes (MS) for filters 1 through 7 with the strobe which inserts the ZVF value into the string of filter responses.

If we were to use the weather threshold directly as a threshold, it would result in comparing the present signal to something generated from the previous 16 range gates. Since it is desired to have the threshold represent 16 gates centered on the gate of interest, it is necessary to pass the input signals

through an 8-gate delay line shift register. The signals emitting from this register then represent returns from the ninth gate of the group used to make the threshold. The signal from this 8-gate delay is also used to form the clutter threshold and map which causes an apparent offset of nine gates in range. This is not important, however, because any target reports sent to the IOP computer contain the range number pertaining to the gate in which the signal actually appeared.

D. Video Generator (Not required for automatic operation)

In many cases it is desirable to display the pattern of weather in the area of coverage. Present ASR's do not completely discriminate between weather and targets, but the MTD eliminates the weather clutter. To provide a synthetic video presentation of weather, a separate circuit was installed whose output is applied to the DEDS display console via the spare video input port. Figure 20 is a block diagram of this circuit.

An integrated circuit memory is used to store the signals for presentation because the video must be displayed on every scope sweep but is only generated once for each CPI (10 sweeps). By combining three range gates into one signal, the information from the 760 range gates can be stored in a 256-word memory. The outputs from the seven non-zero filters in three consecutive gates are totaled in an adder. The number of leading zeros in this 15-bit word is noted and expressed as a 4-bit number. The 1's complement of this 4-bit number is a logarithmic representation of the total weather return in the three gates and is stored in the memory.

The memory is read out to the scope via a 4-bit digital/analog converter (DAC) at a 434-kHz (1.3 MHz/3) rate once each sweep. A new piece of information

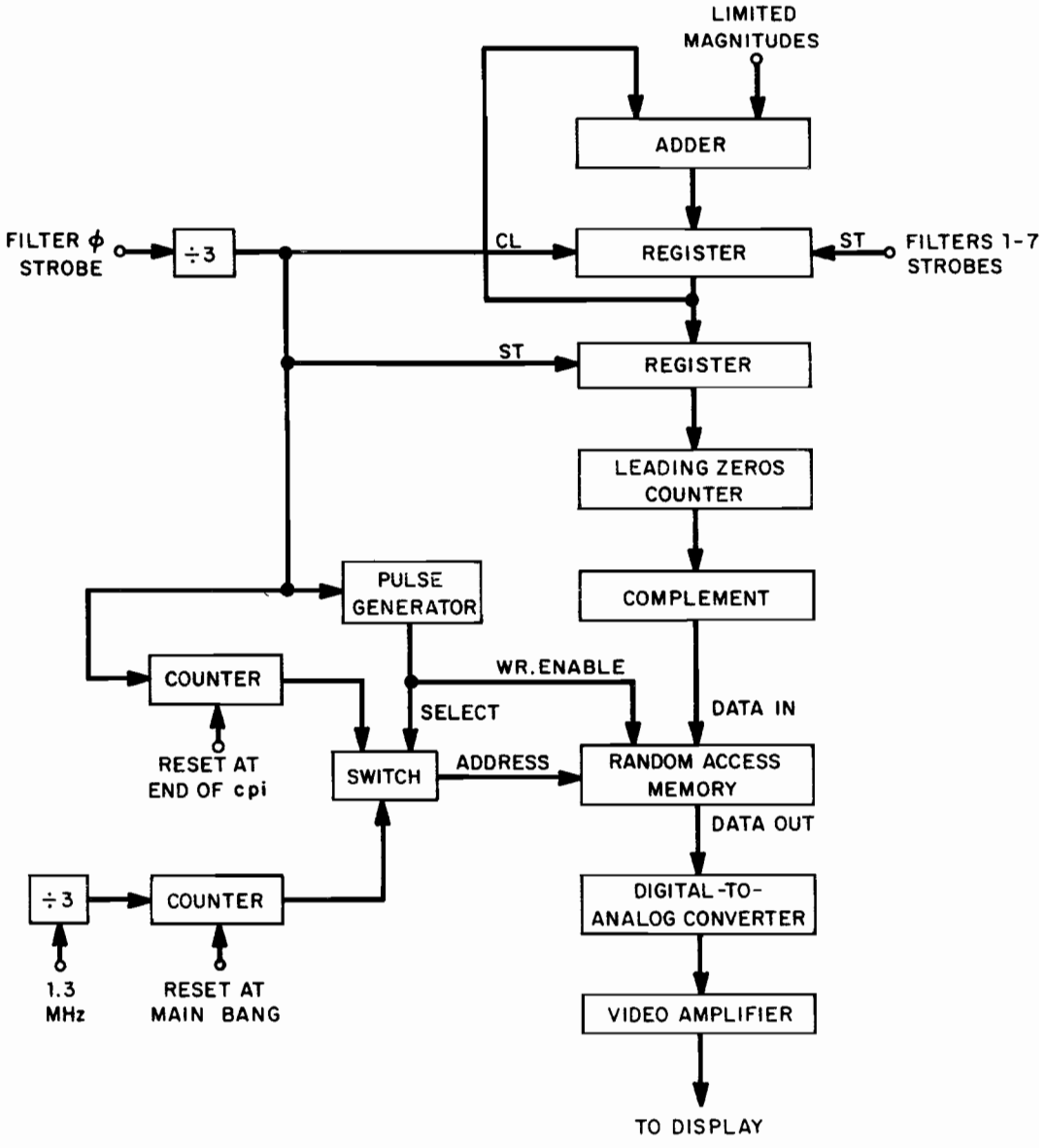


Figure 20 - Synthetic MTI Video Generator Block Diagram

is generated at the memory input each 23 microseconds so the entire 256 words are replaced every 8 milliseconds (1 CPI). Two address counters are used for the memory. The fast one counts at 435 kHz for the output display and the slow one counts at 43 kHz for proper location of the input data. Whenever a new piece of information appears at the memory input a pulse is generated which selects the slow address counter and causes a write enable signal to occur. This process takes less than 100 nsecs so the momentary loss of output on the display is not noticeable.

The entire weather threshold with the exception of the video generator is located in the upper rear-panel of the top side of drawer "D". The video generator is located with the disc interface circuitry below drawer "D".

XII. CLUTTER THRESHOLD GENERATOR

The clutter threshold generator is shown in the block diagram of Figure 21. The filter value stream from the magnituder is applied to the input of a register and the zero velocity filter (ZVF) strobe causes the zero filter values to be picked out and stored. The value of the clutter map for the range/azimuth cell of interest is called up from the disc memory and put into a recursive filter along with the new clutter value for that cell. This filter, made up of adds, negates and shifts, implements the algorithm $X = (M - N) - \frac{1}{2^n}(M - N) + N$, where $\underline{M}$ represents the map value, $\underline{N}$ the new value and $\underline{n}$ the filter time constant. For $\underline{n} = 3$, the effect of the circuit is to add 1/8 of the new value to 7/8 of the stored map value. The output of the recursive filter becomes the new updated map value and is stored back onto the disc. A time delay circuit is included which bypasses the filter causing the map to be filled with new input

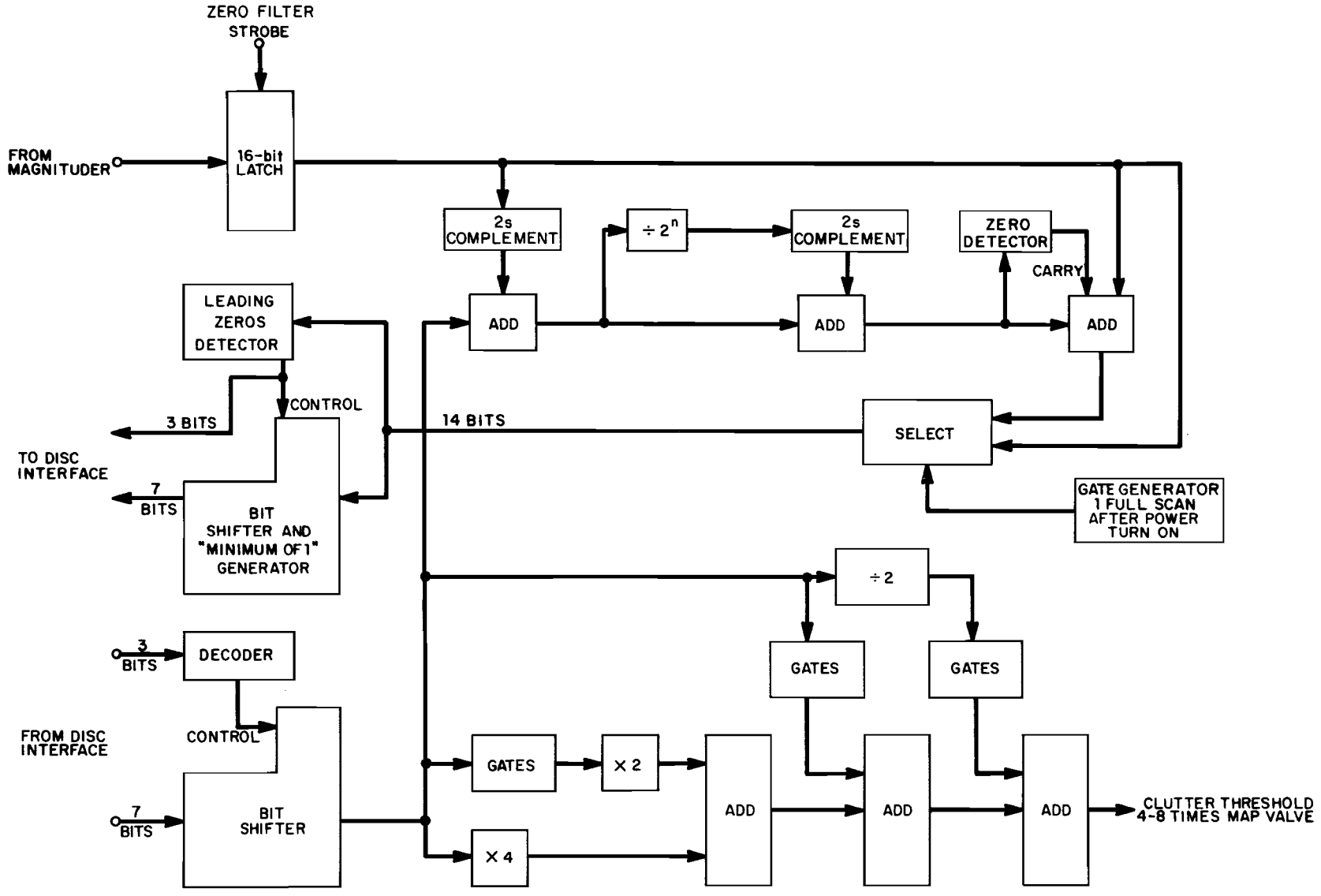


Figure 21 - Ground Clutter Threshold Generator Block Diagram

data when power is initially applied to the MTD. Without this feature for large values of n the map might take an inconveniently long time to stabilize.

The number stored in the map is made into a threshold value by multiplying it by a factor of 4 through 7 1/2, as in the weather threshold generator. In the present case the number is multiplied by 4 and then augmented by any or all of 2, 1, 1/2 times the number. Both the filter time constant, n, and the multiplier factor are selected by inserting patch plugs on connectors in the lower rear panel of drawer "D". After the data has been strobed into the input register, the remainder of the generator has no timing and operates on the "ripple" principle.

Since the disc can store only 10-bit words and the recursive filter output contains 14 bits, a converter to floating point arithmetic and back is employed. The word is examined starting with the most significant bit and the number of zeros to the left of the first 1 is counted. This number can range from zero to seven and is stored on the disc as the first three bits of the 10-bit word. If there are more than seven leading zeros, the number is still 7. The next seven bits are copied exactly into the remaining seven bits of the 10-bit word for storing. When the number is read from the disc the process is reversed with the seven data bits being placed in the 14-bit word along with the correct number of leading zeros as specified by the first three bits of the floating point word. Note that the precision of the 14-bit word has been truncated to seven bits in the process of conversion.

If the number to be stored on the disc is identically zero, the least significant bit is forced to a 1 in order that we may never have a threshold setting of zero in the system.

The clutter threshold generator is located in the lower rear panel of drawer "D" with the exception of the fixed-floating-fixed point converter which is located with the disc interface and controller on the panel in front of the disc.

XIII. DISC MEMORY CONTROLLER AND INTERFACE

The function of the controller is to provide the track address and write enable lines for the disc and the clocks necessary to transfer data to and from the disc. It must also contain a parallel-to-serial and serial-to-parallel converter since the words are stored on the disc in serial bit form. The function of the interface is to transfer data to and from the disc using the timing pulses generated by the controller. To accomplish this it is necessary to store data for one full disc write/read operation plus the maximum disc access time. Figure 22 is a block diagram of these circuits.

A. Interface

Blocks of data containing clutter map information for four CPI's are transferred to and from the disc. Two buffers, each consisting of a 3072-word MOS shift register, are used in a "ping-pong" configuration. These integrated circuits are TTL compatible static-type MOS devices. During the time interval that encompasses four CPI's one buffer is unloaded onto the disc and then refilled from the disc with new information. The other buffer is temporarily interfaced to the recursive filter described in the clutter threshold generator. The map value for a given cell is taken from the output end of the shift register, updated in the filter and inserted at the input end of the same shift register as the next cell's data is withdrawn from the output. After four CPI's all the data originally in the register has been replaced with new

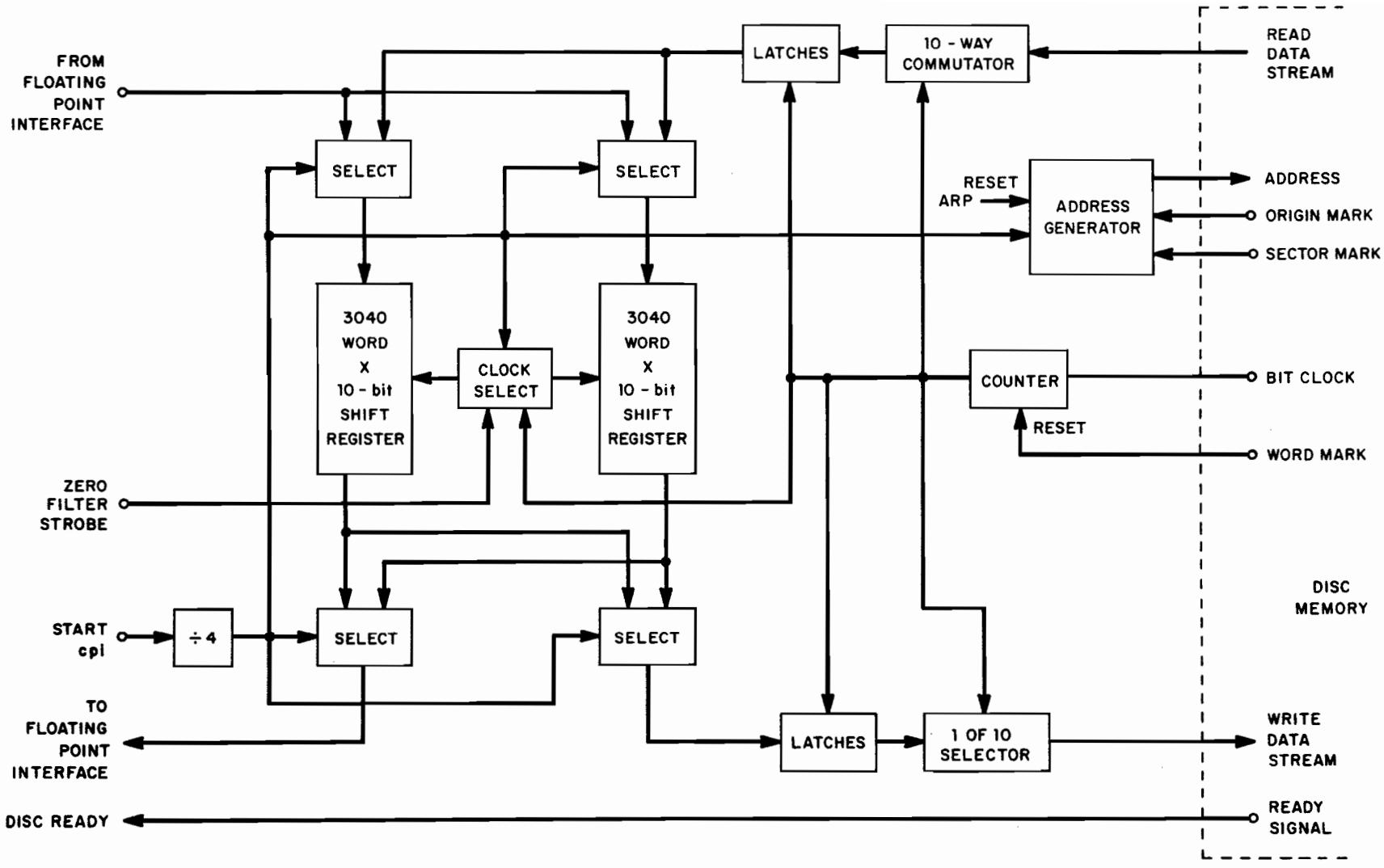


Figure 22 - Disc Interface Block Diagram

data and the buffers are exchanged. For example, as CPI's number 5-8 are processed in buffer A, buffer B is storing away on the disc the updated data for CPI's numbered 1-4 and fetching previous scan map data from the disc for CPI's numbered 9-12.

Three clocks are used with the MOS buffers. The clock for the buffer connected to the recursive filter is the zero filter strobe (ZST) so that signals move along the register one notch each time a range gate is processed. The buffer interfaced with the disc uses disc read and write clocks generated by the disc controller. In addition, a train of 32 pulses is added to the ZST clock string at the beginning of each 4-CPI group because the registers are 3072 words long and 4 CPI's contain 3040 range gates. This clock inserts 32 dummy words into the register so that data can circulate completely. The time interval necessary to process 4 CPI's is nominally 39 milliseconds while the time interval to write and read four CPI's on the disc including worst-case access time is 36 milliseconds, so the registers are always ready for switching at the end of four CPI's.

B. Controller

The disc surface is configured into 64 tracks of eight sectors each. Each group of four CPI's occupies four sectors or 1/2 a track, so each track is addressed in two halves starting at the disc origin mark, a reference point permanently recorded on the disc. There are, therefore, 128 addressable portions of the disc, of which 120 are used to store map data for the 480 CPI's in an antenna scan. The normal operation of access/write/read is kept to a maximum of 36 milliseconds by allocating the space in such a way that the write and read operations occur on consecutive half-tracks, thus requiring no access

time between them. If we let each track have an A-half and a B-half and let the CPI groups be numbered from 0 to 119, then the assigned space is as shown in Table 8. At the start of any A- or B-half a new track can be addressed. Table 9 shows the order of write/read operations. Note that the write/read operation never includes two A-halves or two B-halves.

Each time the buffers are switched a new 1/2-track address is generated for the write operation. Upon completion of the write operation, the address is incremented by one for the read operation. The location of the A-half of a track is identified by the disc origin mark. The location of the B-half of a track is identified by the start of the fifth sector in that track. When the proper 1/2-track address has been located, taking up to a maximum of 18 milliseconds or one revolution, the write enable line is set and the write clock is turned on to strobe 30720 data bits onto the disc. This represents 3072 10-bit words or 3040 real words and 32 dummies. The parallel-bit words are fed through a selector that picks up each bit in turn to form the serial stream to the disc.

Having completed the write phase, the address counter is incremented and the read clock is turned on to strobe 30720 data bits back into the shift register via a serial-to-parallel converter. The read clock must be delayed 16 bit-times to allow the passage of some preamble bits used by the disc in bookkeeping but not relevant to the data. For details of disc operation, please refer to the Digital Development Corporation instruction manual.

The disc interface and controller are located in a panel mounted behind the cover in front of the disc itself.

XIV. THRESHOLD DETECTORS

Figure 23 is a block diagram of the threshold detectors. Information from the magnituder is delayed eight range gates by means of a 64-word shift

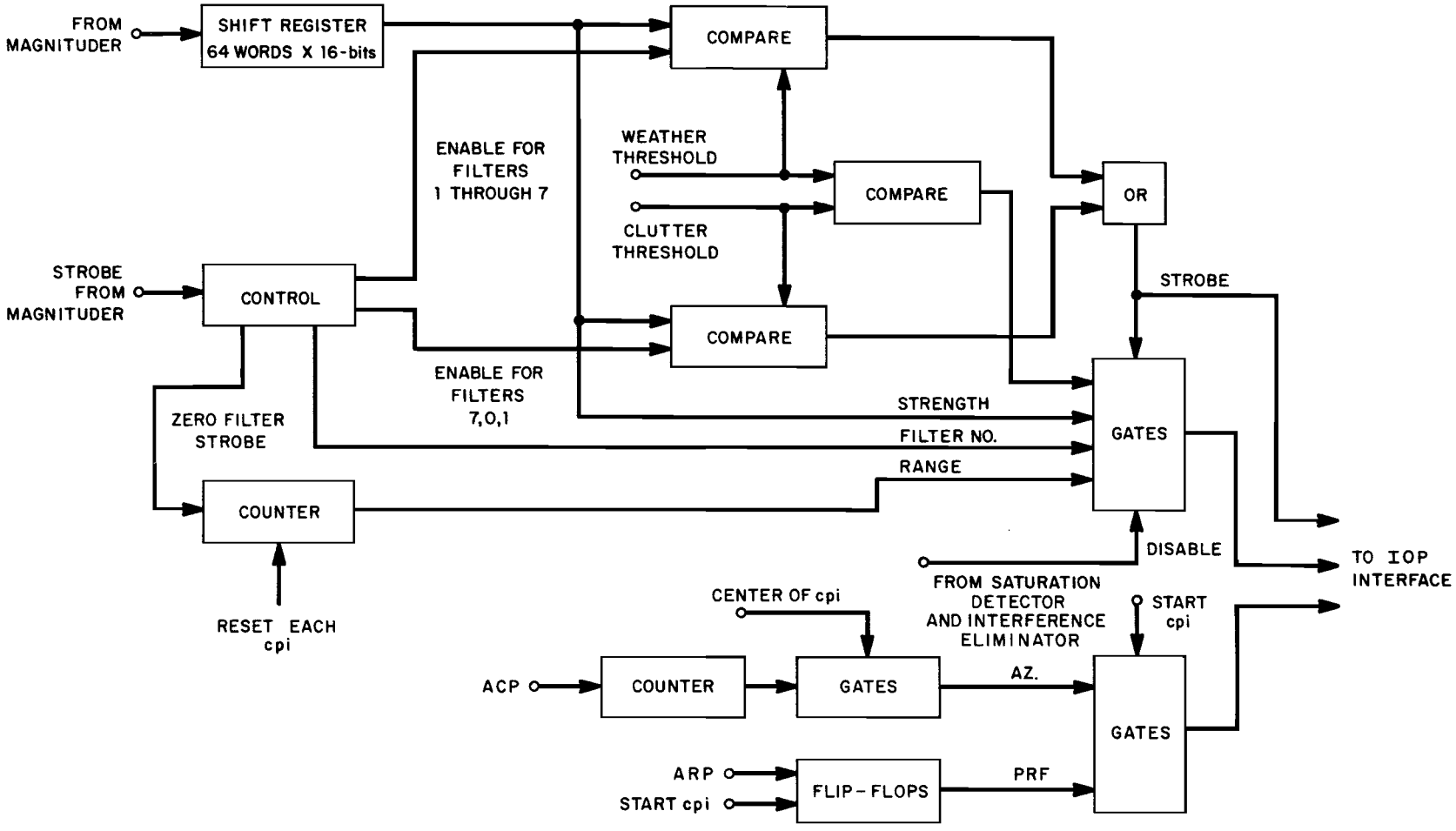


Figure 23 - Threshold Crossing Detector Block Diagram

TABLE 8

CPI STORAGE LOCATIONS ON DISC

CPI Group Number	Disc Location
0	0A
1	30A
2	0B
3	30B
4	1A
5	31A
6	1B
7	31B
8	2A
9	32A
10	2B
11	32B
12	3A
13	33A
14	3B
15	33B
16	4A
17	34A
.	.
.	.
.	.
116	29A
117	59A
118	29B
119	59B

TABLE 9

DISC ADDRESS GENERATION

Buffer Number	Write Address	Read Address
1	0A	0B
2	30A	30B
1	0B	1A
2	30B	31A
1	1A	1B
2	31A	31B
1	1B	2A
2	31B	32A
1	2A	2B
.	.	.
.	.	.
.	.	.
1	28B	29A
2	58B	59A
1	29A	29B
2	59A	59B
1	29B	0A
2	59B	30A

register. The purpose of this delay is so that the filter values from any given gate will be thresholded against a number which is the average of 15 gates centered around the gate of interest (see weather threshold generator). The input data for the clutter threshold generator is also taken from the output of this delay line. Whenever a signal exceeds the threshold value applied to a particular comparitor, its output is a logical one. The output of the ZVF to clutter comparitor is forced to be a one for all filter times except zero, when it depends on the signal. The output of the signal to weather comparitor is forced to be a one for the zero filter time only. Filters 1 and 7 are also thresholded against an attenuated version of the clutter signal to take care of clutter spillover into these filters. The amount of this attenuation is set by a patch plug on the lower rear panel of drawer "D". The output of this comparitor is forced to be a one for all but filter times 1 and 7. When and only when the outputs of all comparitors are one for a given gate and filter time, a threshold crossing is generated and a strobe formed (OUTSTROBE). This strobe gates the proper velocity, range and strength messages to the IOP interface for the signal causing the OUTSTROBE. The strength word is the delayed magnitude and the range word is the output of a counter which counts range gates and is reset each CPI. The velocity is the filter number taken from a counter that counts to eight for each gate.

If there was an output from the saturation detector or interference eliminator circuits associated with a given range gate, THRESHSTROBE is inhibited during the thresholding time for all filters in that gate.

At the start of each CPI a message is sent to the IOP interface which contains an indication of the prf of the radar during that CPI and the azimuth of

the center of the CPI. There are also two status bits in the message which provide information about the data transfer to the previous CPI. If bit 1 is high it is an indication that the input buffer to the IOP interface receive more than the 38 threshold crossings it can handle per CPI and that some hits were lost. If bit 2 is high the IOP has not completely emptied the output buffer of the IOP interface before the start of the next CPI, also causing a loss of data.

The threshold detectors are located in the lower rear panel of drawer "D".

XV. IOP INTERFACE

Figure 24 is a block diagram of the IOP interface. At the beginning of each CPI, switches select the azimuth and prf (PAS) word and it is strobed into a register. The selectors are then switched to pick up any velocity/range/strength (VRS) words that may be accompanied by an OUTSTROBE. The register is attached to the input of and forms the first stage of a 40-word by 32-bit shift register. When any VRS word is loaded into the register by an OUTSTROBE the previous word from the register is shifted down the shift register. This shift register holds a PAS word and up to 38 VRS words without filling and setting status bit 1. At the end of the CPI a clock running at 1.3 MHz shifts the words through the remainder of the input register and through the output register until the PAS word lies at the end of the output register. An input data request (IDR) is then issued to the IOP computer. When the IOP acknowledges receipt of the word the output register is shifted along one word, and another IDR pulse generated. This continues until the output data register is empty. Should another CPI be completed prior to the emptying of this register, status bit 2 is set. While the IOP is emptying this register the input register is being refilled with data from the next CPI.

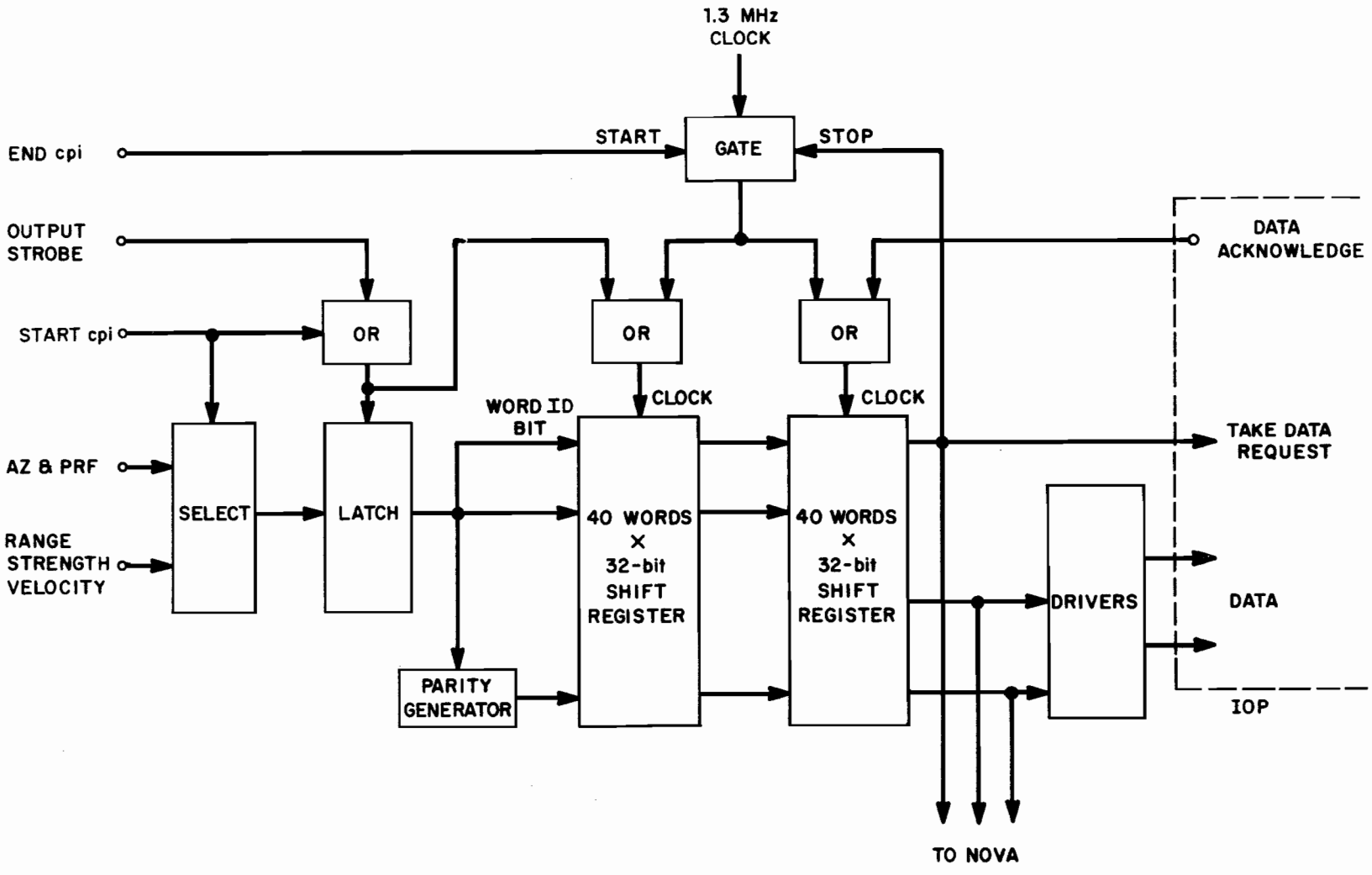


Figure 24 - Output Interface Block Diagram

The output data lines and the IDR pulses are also sent to the NOVA test computer interface located in drawer "A", but no handshaking takes place. It is up to the NOVA interface to read the data before another IDR is issued.

The IOP interface is located at the right side of the inner and outer upper rear panels in drawer "D".

XVI. TEST MEMORY AND CONNECTION (Not required for operation)

Drawer "B" contains the test memory which receives information from the NOVA interface and stores simulated input data for an entire CPI. If the toggle switch on the rear of the drawer is in the TEST position, 11-bit I&Q words are directed into the main 8K memory in place of data from the A/D converters. Since the test memory contains only one CPI of data, each CPI receives the same input information and the output of all processed CPI's is identical until the contents of the test memory is changed. A NOVA program has been written to load the test memory via the interface with new data once per antenna scan and examine the MTD output as it is received back from the IOP interface. In this way a complete closed-loop test system is operated.

The NOVA interface also handles the single-gate data for the spectrum analysis program.

APPENDIX A

SITE ADAPTATION ALIGNMENT

The adjustments on the MTD are composed of switches and patch plugs. All can be classified as "one time" adjustments because once they are programmed for a given radar site, no further changes should be necessary. The patch plugs are all located in the lower rear of drawer "D" and perform the following functions:

Location	Function
XJ1	Recursive filter time constant control
XJ2 (left end)	Weather threshold level (filters 2-6)
JJ2	Weather threshold level (filters 1&7)
XJ2 (right end)	Clutter threshold level
YJ2	Clutter threshold level ratio for filters 1 & 7

The plugs for XJ1 and YJ2 are to be installed with the identifying label front. The threshold level plugs are to be installed with the "W" and "C" labels to the front.

Three plugs are supplied for the filter time constant which allows a time constant of 8, 16 or 32. These numbers mean that the amount of new data added to the threshold each scan is 1/8, 1/16 or 1/32 or the new data value.

The threshold level plugs are to set the multiplier factor applied to the threshold. These plugs range from factors of 4 through 7 1/2 in increments of 1/2 for clutter and from factors of 3.5 through 6.56 for weather. Note that there are no plugs supplied for the highest setting as this is the default value.

The clutter threshold ratio plug controls the amount of clutter threshold applied to filters 1 and 7 to take care of clutter spreading due to antenna scanning.

Plugs are available for 30 dB, 36 dB and 42 dB ratios. For example, if the 30 dB plug is installed, the ratio of clutter threshold applied to filters 1 and 7 to clutter threshold applied to filter zero is -30 dB. The plug does not affect the weather threshold applied to filters 1 and 7 in any way.

Figure 25 shows the layout of the switches located in drawer "D" positions R17, R21, R22. In each position the rear-most switch of the group of eight is not used and has been disabled. As shown in Figure 25, the switches in position R17 perform two functions. The STC attenuator located in the radar front-end is reduced from an initial value as the negative fourth power of range in 1 1/2 dB steps. The initial value is set by the nearest six switches of R17, the closest switch being the least significant bit. Pushing down on the left side of a switch rocker increases attenuation.

The seventh switch from the front of R17 controls the prf stagger. Pushing down on the right side of the switch rocker causes the prf to go to the average number (no stagger), but this average value prf will still jitter on a scan-to-scan basis.

The nearest seven switches of position R22 and switches 5, 6 and 7 of position R21 are used to control the position of the selected range gate used in the SGP routines and also to position the range of the test target. The bit positions are as shown in Figure 25 and the increment is 1/16 of a mile. Pushing down on the left side of a switch rocker increases the range of the gate.

The switch nearest the front of R21 controls the scan-to-scan prf jitter. Pushing down the right side of the rocker disables this jitter. Note that this switch in no way affects the CPI to CPI prf stagger. The second switch

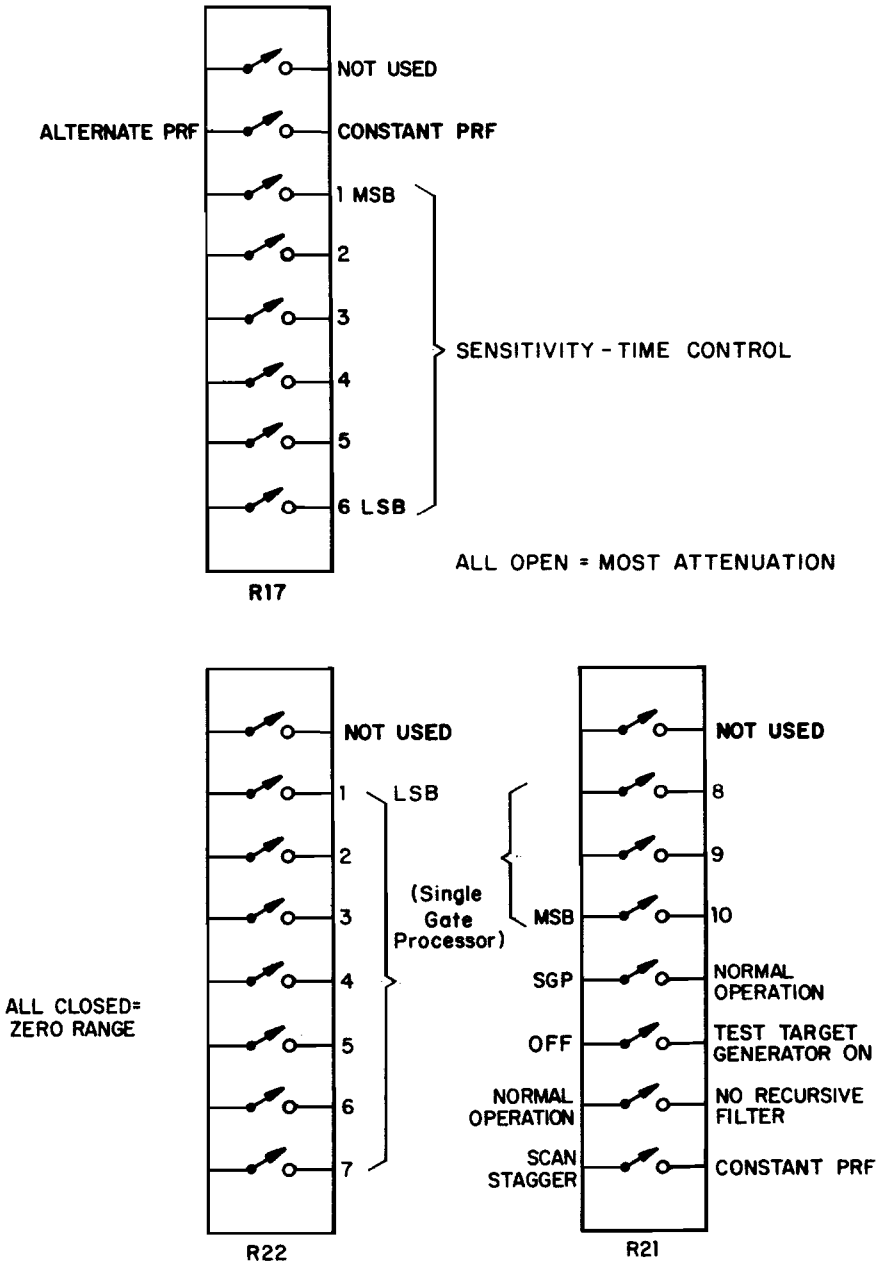


Figure 25 - Control Switch Function Diagram

from the front of R21 causes the recursive filter in the clutter map circuitry to be bypassed. This is useful when troubleshooting as changes in the clutter threshold are immediately visible in the map output. Pushing down on the right side of the rocker diasbles the filter.

The third switch from the front of R21 controls the test target generator excitation pulse. Pushing down the right side of the rocker turns on the test target. The fourth switch from the front switches the input processing into continuous operation for SGP use. This switch must be pushed to the left for SGP and must be pushed to the right for normal or test operation.

A slide switch located on the front top outrigger board of drawer "D" selects the source of the output data acknowledge signal. It should be set to IOP for normal operation. When the Univac program is not running, it should be set to NOVA to allow transmission of output data to the NOVA computer and the local DEDS display console.

APPENDIX B

CHECKING AND TESTING

To facilitate checking the system, sockets for 10-bit digital-to-analog converters (DAC's) have been liberally installed throughout the equipment. Several DAC's are permanently in place and others are provided to be installed when required. Two DAC's are mounted in the top rear center area of drawer "C" and are connected to the input of the reordering memory. Three units are mounted in the lower rear panel of drawer "D", but their outputs are brought up to the front for easy access. The remainder of the units are mounted on two outrigger panels attached to the upper and lower front panels of drawer "D". Pattern 14 of the upper outrigger is a collection of output points for all the DAC's on that outrigger plus those buried in the lower rear panel. Table 10 lists the details of the DAC locations and test points.

The test memory is used to check the entire signal flow through the MTD with the exception of the input processing. A digital ramp generator known as a "bit-box" is used to test that. A complete check of the system includes the following procedure:

Connect the bit-box to the input of the MTD in place of the 10 I-bits and 10-Q bits from the A/D converters, leaving the encode command and data ready lines connected normally. Connect the LOAD and COUNT wires from the bit-box

TABLE 10

LOCATION OF DAC TEST MODULES

DRAWER "C"

DAC Location	Signal Output Pin	Ground Pin	Signal Description	Most Significant Bit
*Top center of drawer	3	6	Memory input - I	Bit 10
* Top center of drawer	3	6	Memory input - Q	Bit 10

DRAWER "D" Upper Outrigger

DAC Location	Location 14 Signal Output Pin	Location 14 Ground Pin	Signal Description	Most Significant Bit
49	15	8	Memory input - I	Bit 10
37	13	8	Memory input - Q	Bit 10
50	16	8	Canceller output - I	Bit 12
38	14	8	Canceller output - Q	Bit 12
*U15	10	8	Threshold input	Bit 15
*U5	9	8	Clutter threshold	Bit 14
*UU-11	11	8	Weather threshold (fine)	Bit 9
*UU-1	12	8	" " (coarse)	" 19

DRAWER "D" Lower Outrigger

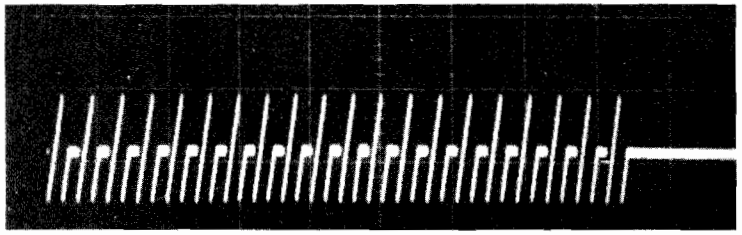
DAC Location	Signal Output Pin	Ground Pin	Signal Description	Most Significant Bit
13	3	6	DFT output - I	Bit 15
14	3	6	DFT output - Q	Bit 15
25	3	6	Weighted output - I	Bit 15
26	3	6	Weighted output - Q	Bit 15
27	3	6	Magnitude w/o ZVF	Bit 15

*Permanently installed

to points M12-6 and P27-1 respectively of the timing section in drawer "D". The N/T switch on the back of drawer "C" must be in normal. Set the toggle switches on the bit-box so that the most significant bit is a 1 and all other bits are 0's. Attach a scope probe through the small filter provided to the DAC's on the input of the 8K memory in drawer "C", and trigger the scope on the burst trigger. The filter consists of a capacitor of 180 pF from signal to ground to decrease the transients at the DAC output. Each DAC output should be a sawtooth waveform with 20 teeth as shown in Figure 26a. Each "tooth" extends from zero to maximum (1023) and then repeats the first half again. This is because the bit-box is counting at 2.6 MHz (twice the range gate frequency) and goes through 1520 counts in 760 range gates. There should be no reversals of direction in the ramps at the DAC outputs, and the slope should be smooth and straight.

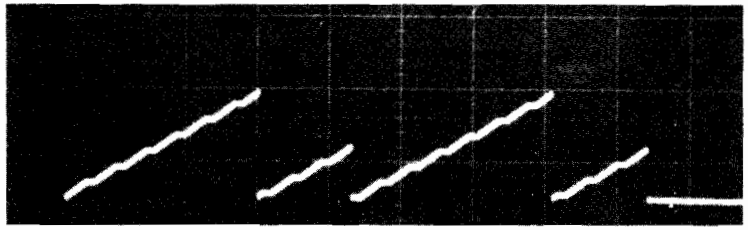
The probe (meaning probe and filter throughout this entire procedure) should next be attached to pattern 14, pin 15 on the upper outrigger of drawer "D". Insert the DAC into location 49 and the output waveform should be as shown in Figure 26b. Move the DAC to location 37 and observe the signal at pattern 14, pin 13. It should be the same as the previous signal. When moving the DAC around care must be exercised to see that it is properly oriented in the socket. This completes the tests using the bit-box. Reconnect the A/D converters and set the N/T switch to TEST in preparation for loading the test programs from the NOVA computer.

Two test programs have been written for use with the MTD. These have been thoroughtly documented in memos by R. D. Lewis: 43M-200 "Sine-wave Data Test Program MTD-0006 Revised and 43M-219 "MTD Aux Memory Tester, RAMP.



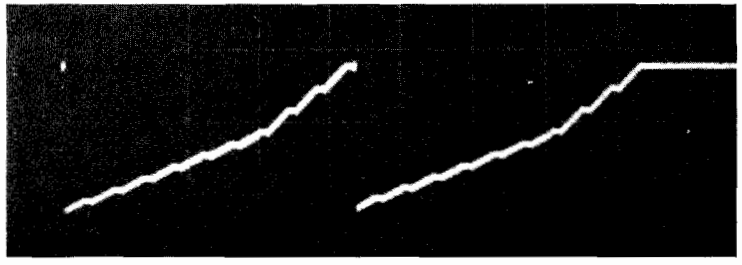
MEMORY INPUT w/ BIT BOX

(a)



MEMORY OUTPUT w/ BIT BOX

(b)



MEMORY OUTPUT WITH NOVA RAMP

(c)

CLUTTER THRESHOLD WITH NOVA RAMP

(d)

Figure 26 - Ramp Test Waveforms - 1

Load program number 0025. RB and start at NOVA location 3, thus loading the positive ramp into both I&Q sections of the test memory. This ramp starts at zero level and is incremented one count in amplitude each range gate until gate #511, then incremented two counts per gate throughout the rest of range. The ramp therefore has a slope of 1 for the first 2/3 of range and a slope of 2 thereafter. The signal represents DC levels in each gate with increasing amplitude and with no AC components.

Each memory output (pins 15 and 13 of position 14 on the upper outrigger) should present the waveform shown in Figure 26c. After allowing a few minutes for the recursive filter to build up observe pin 9 of pattern 14. The waveform is the filter output and should be like that shown in Figure 26d. It should be absolutely steady once the filter has stabilized. Note that Figure 26 shows two complete CPI's in each photo and that the timing was strapped to constant prf when the pictures were taken. If tests are made in the variable prf mode, the first CPI will be expanded in time and the second CPI will be compressed.

Next, the AC ramp should be loaded by restarting the NOVA at location 2. This signal is a sinewave designed to fall into filter #4 with an amplitude that increases monotonically just as the previous ramp did. The memory outputs should look like Figure 27a, b. Note that the signal in the Q channel is always zero. Now observe the output of the three-pulse canceller by inserting the DAC into locations 50 and 38 and probing location 14, pins 16 and 14 respectively. The waveforms should be as shown in Figure 27c, d. Next, move the DAC to the lower outrigger panel positions 13 and 14 and observe pin three of each position. The real and imaginary parts of the discrete Fourier transform

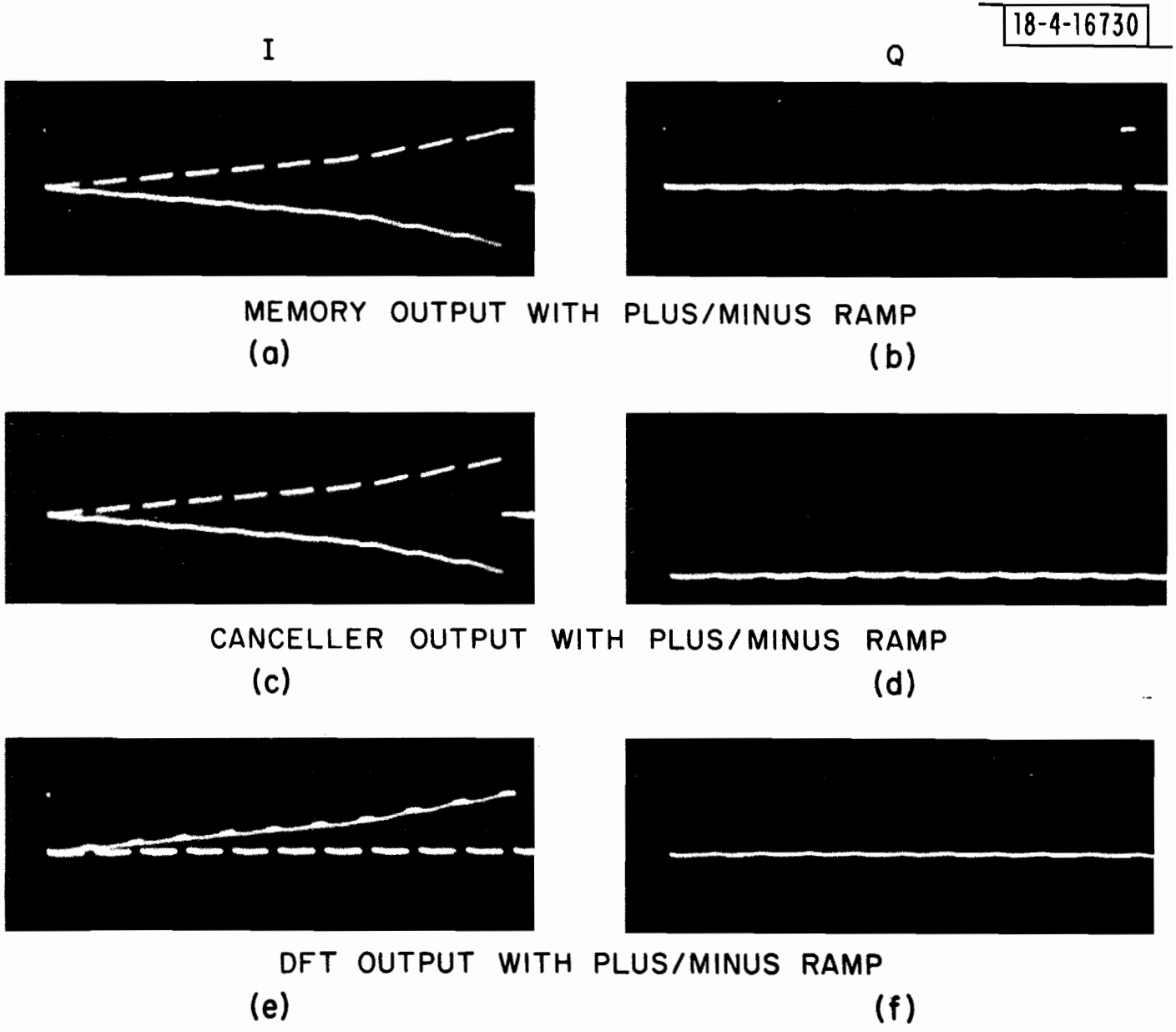


Figure 27 - Ramp Test Waveforms - 2

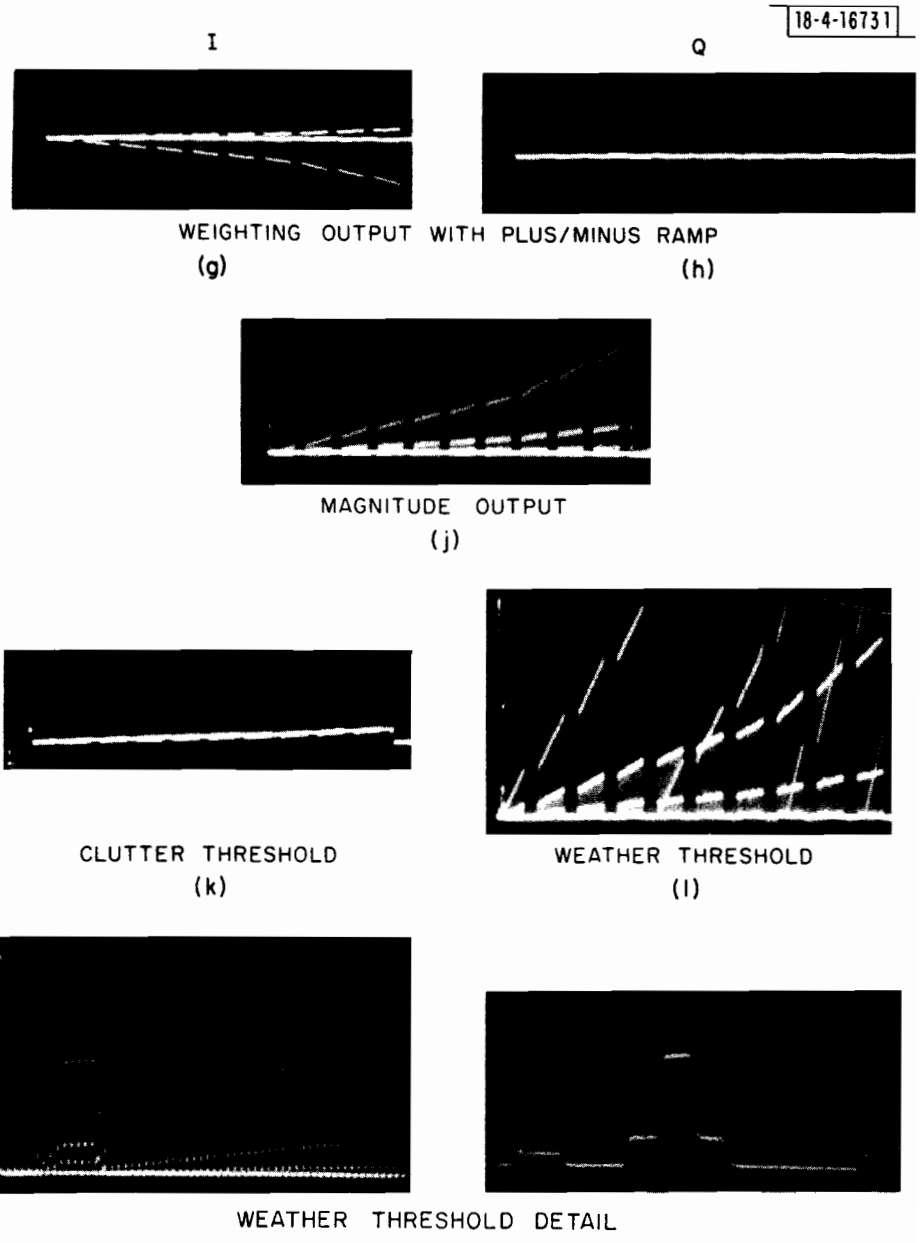


Figure 27 - Ramp Test Waveforms - 2

output appear here and should be the same as in Figure 27 e, f. After passing through the weighting circuits, the outputs are on pins three of locations 25 and 26 and should look like Figure 27 g, h. Note that the signal is inverted at this point. The output of the magnitude circuit, location 14, pin 10 of the upper panel, should look like Figure 27 j. The clutter and weather thresholds should appear as in Figure 27 k, ℓ. Figure 27 m is an expanded view of the first part of Figure 27ℓ and Figure 27 n is a further expanded portion showing one range gate. It can be seen that the signal spills over into filters three and five and also has a DC component. The three apparent ramps in Figure 27m are caused by the accumulation of these various components with the largest ones building to a high level first. By changing the contents of NOVA location 4 to 5001_8 and restarting the program at location 2 the I&Q waveforms are interchanged. This should be done because the all-zero signal in one channel is not terribly enlightening. This completes the tests using the ramp signals. Any deviation from the exact waveforms in the photos is a sign of a malfunction and should be investigated.

The second program (MTD-0006) should be loaded into the NOVA and then into test memory according to the instructions in the Lewis memo. This program puts eight different sinewaves into eight consecutive range gates starting at gate #16. These sinewaves are at frequencies of 1/8, 1/4, 3/8, 1/2, 5/8, 3/4, 7/8 and 1 times the radar prf thus furnishing a sinusoid centered in each of the eight Doppler filters. Figure 28 shows the ten consecutive sweeps fed into the memory for the I&Q channels. Figure 29 contains all the rest of the waveforms for this input signal. Since these sinewaves all have a peak amplitude of 1023 units and the saturation detector inhibits signals larger than 959 units,

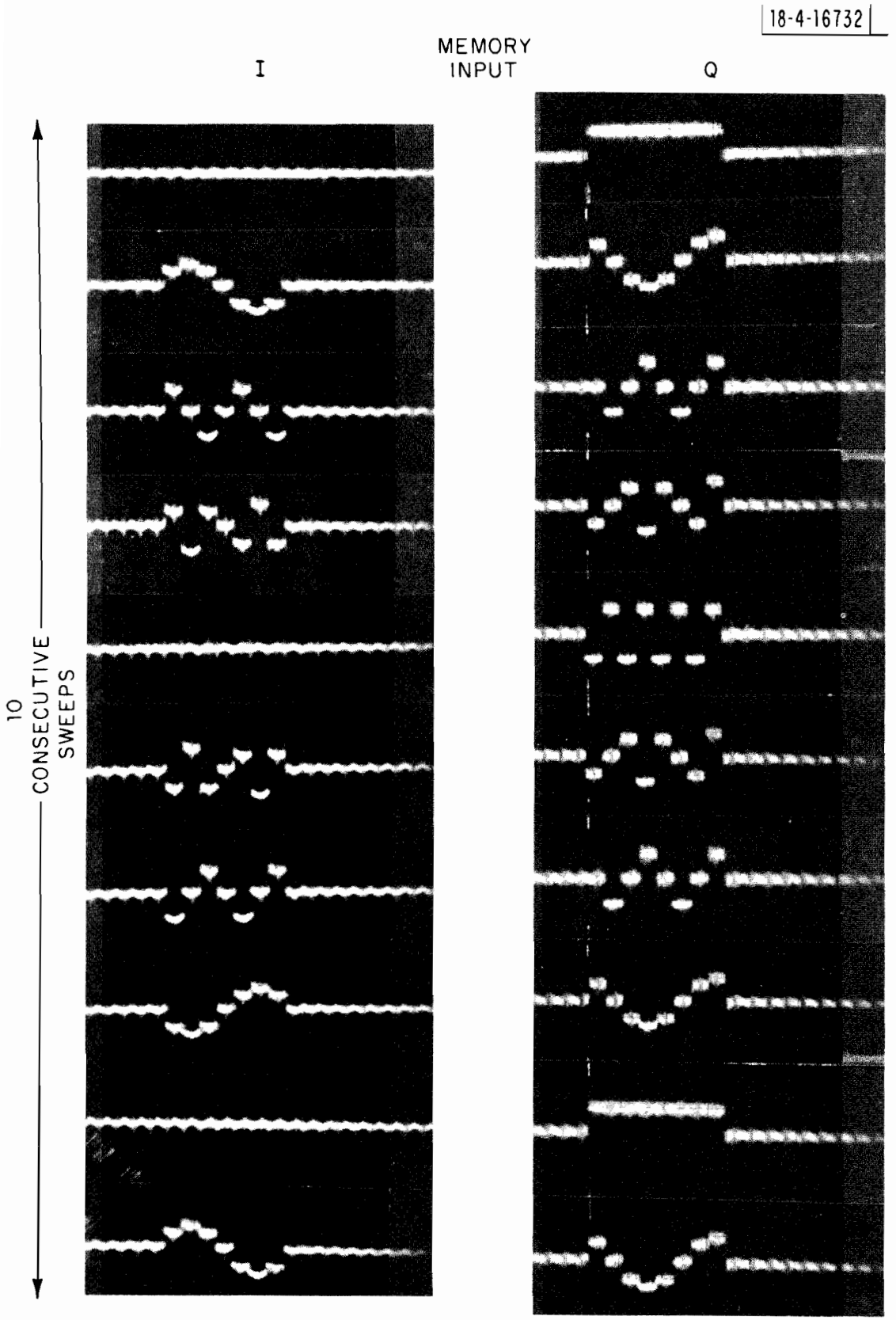


Figure 28 - Sinusoid Test Waveforms - Input

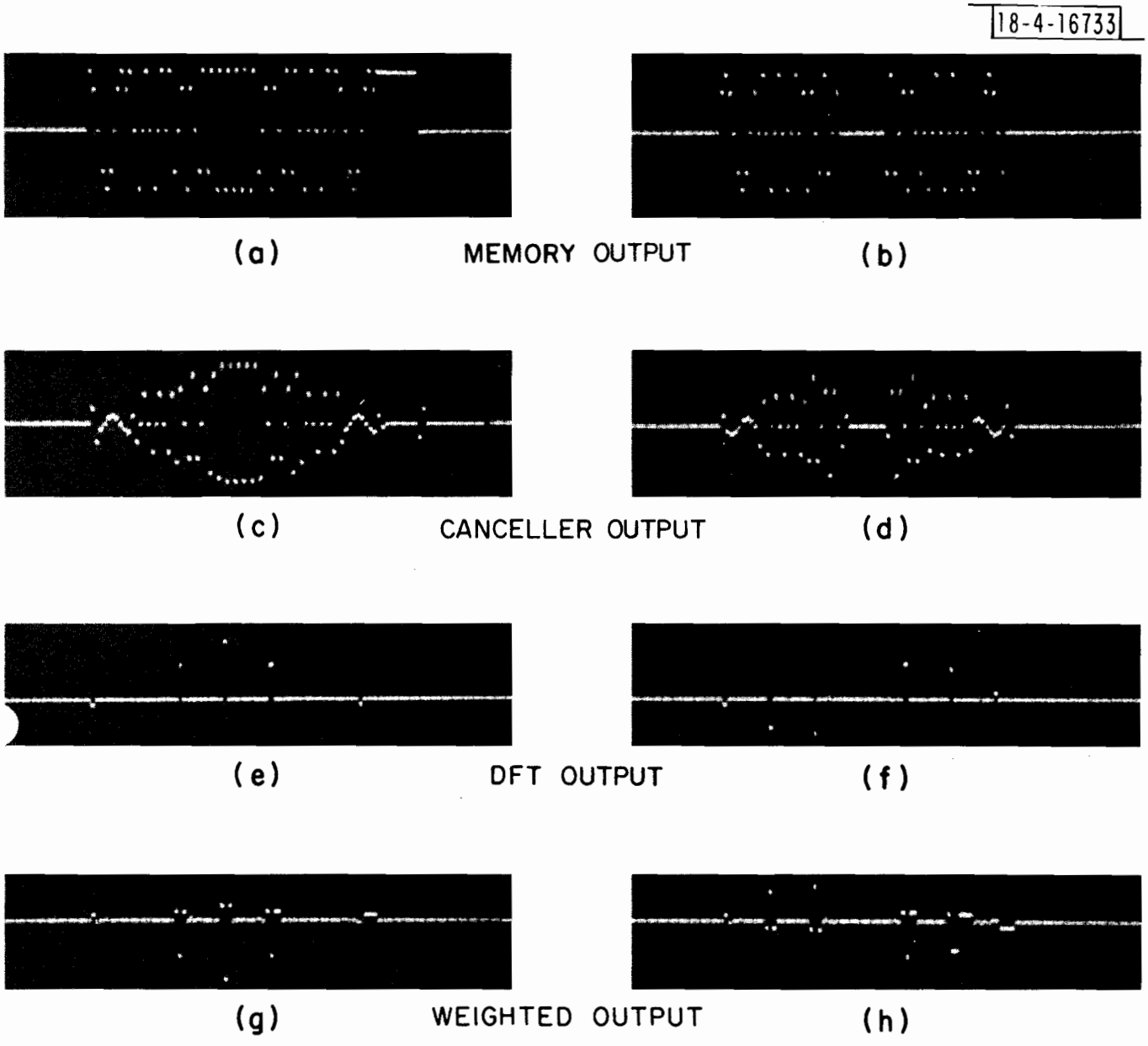
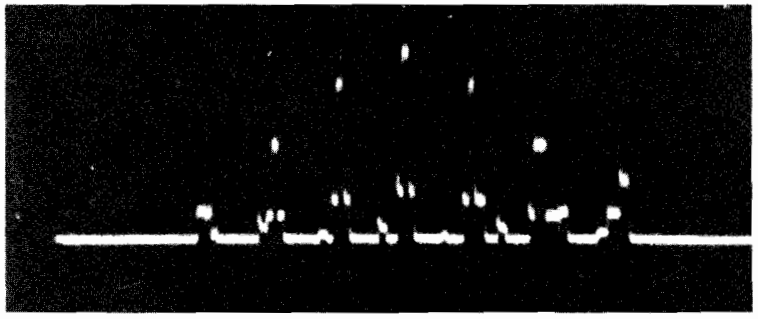
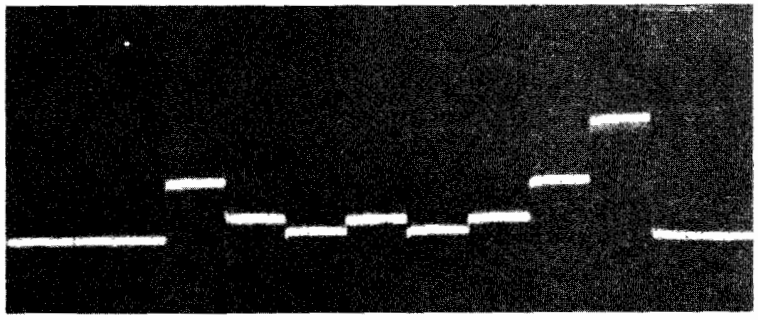


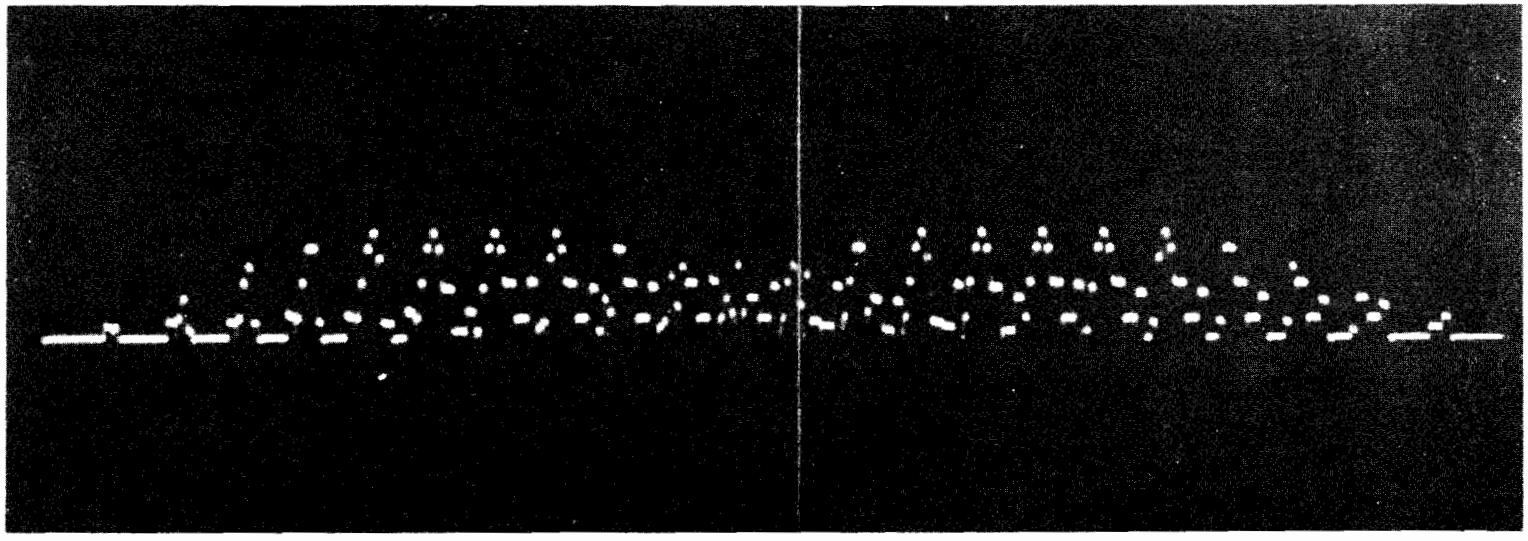
Figure 29 - Sinusoid Test Waveforms - Output



MAGNITUDER OUTPUT
(j)



CLUTTER THRESHOLD
(k)



WEATHER THRESHOLD
(l)

Figure 29 - Sinusoid Test Waveforms - Output
(Cont.)

none of the output reports will be passed to the IOP computer or NOVA unless the saturation detector is disabled by installing a Berg clip between pins 2 and 7 of pattern 14 on the upper outrigger. With this jumper in place, one should observe 19 strobe pulses per CPI at pattern 14, pin 3. These strobes are used to transfer information to the IOP and represent one PAS word and 18 VRS words in this case. If all waveforms are exactly like those in the photos, the MTD is in working order.

One other program, the so-called "38 targets" is included on the sinewave tape. This may be loaded by following the instructions in the Lewis memo. The 38 targets are more or less equally distributed over the entire radar range and are centered in filter zero. Since the clutter threshold would soon charge up and inhibit their transmission to the IOP, it is necessary to disable the clutter threshold with a Berg clip between pins 4 and 7 of location 14 on the upper outrigger. The system program should now be loaded into the NOVA and the 38 targets should be displayed in each CPI on the DEDS display screen. This is a valuable test of the software because it strains the system to its utmost.

After completing the series of tests one must be sure to return the normal/test switch to NORMAL for use with the radar.

There are three signals brought to the front of drawer "D" on BNC connectors. Two of these are the radar trigger and the start-of-CPI trigger for use as scope sync pulses. The third is a marker for the SGP gate position to allow the operator to position it visually to the desired range.