

**Project Report
ATC-34**

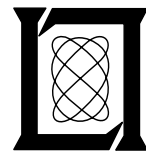
Provisional Data Link Interface Standard for the DABS Transponder

**G. V. Colby
P. H. Robeck
J. D. Welch**

25 April 1974

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS



Prepared for the Federal Aviation Administration,
Washington, D.C. 20591

This document is available to the public through
the National Technical Information Service,
Springfield, VA 22161

This document is disseminated under the sponsorship of the Department of Transportation in the interest of information exchange. The United States Government assumes no liability for its contents or use thereof.

1. Report No. FAA-RD-74-64	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle Provisional Data Link Interface Standard for the DABS Transponder		5. Report Date 25 April 1974	6. Performing Organization Code
7. Author(s) G. V. Colby, P. H. Robeck, J. D. Welch		8. Performing Organization Report No. ATC-34	
9. Performing Organization Name and Address Massachusetts Institute of Technology Lincoln Laboratory P.O. Box 73 Lexington, Massachusetts 02173		10. Work Unit No. (TRAIS) 45364 Project No. 034-241-012	11. Contract or Grant No. IAG DOT-FA 72 WAI-261
12. Sponsoring Agency Name and Address Department of Transportation Federal Aviation Administration Systems Research and Development Service Washington, D.C. 20591		13. Type of Report and Period Covered Project Report	
14. Sponsoring Agency Code	
15. Supplementary Notes The work reported in this document was performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology under Air Force Contract F19628-73-C-0002.			
16. Abstract <p style="text-align: center;">This document specifies provisional data link interface standards for the DABS transponder. It describes the function, timing, and electrical properties of the signals flowing to and from both the Standard Message Interface and the Extended Length Message Interface.</p>			
17. Key Words DABS Transponder DABS Data Link Interfaces		18. Distribution Statement Document is available to the public through the National Technical Information Service, Springfield, Virginia 22151.	
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 24	22. Price 2.75 HC 1.45 MF

PREFACE

The Provisional Signal Formats for the Discrete Address Beacon System have been described in Ref. [1]. The DABS transponder serves not only as a surveillance transceiver but also as a communications modem. Surveillance-related digital processing takes place within the transponder proper, while communications data are transferred between the transponder and associated input/output devices.

This document is intended to define the electrical characteristics of the transponder data interfaces in sufficient detail to allow transponder and input/output device design efforts to proceed independently. Two interfaces exist; the Standard Message interface, designed mainly for flight-related communications; and Extended Length Message interface, which provides an EIA Standard RS-232C [2] connection to available I/O devices for the handling of extended length messages.

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
PREFACE	iii
1. INTRODUCTION/SUMMARY	1
1.1 GENERAL	1
1.2 INTERFACE TYPES AND USES	1
1.3 SM INTERFACE	1
1.4 ELM INTERFACE	3
1.4.1 Uplink Transmissions	3
1.4.2 Downlink Transmissions	3
2. STANDARD MESSAGE INTERFACE	4
2.1 SIGNAL FLOW	4
2.2 ELECTRICAL INTERFACE	4
2.2.1 Logic Convention	4
2.2.2 Clock Line	5
2.2.3 Data Line	5
2.3 SM INTERFACE TIMING	5
2.3.1 Timing Convention	5
2.3.2 Interface Initiation	6
2.3.3 Time and Level Assignments	6
2.4 PBUT AND CAPABILITY INTERFACE	9
2.4.1 PBUT Interface	9
2.4.2 Capability Interface	10
3. ELM INTERFACE	11
3.1 ELM SIGNAL FLOW	11
3.1.1 Uplink	11
3.1.2 Downlink	11
3.2 ELM ELECTRICAL INTERFACE	12
3.2.1 General	12
3.2.2 Data Transfer Rate	12
3.2.3 Signals	12
3.3 ELM INTERFACE TIMING	12
3.3.1 Uplink Interface	12
3.3.2 Downlink Interface	15
REFERENCES	17

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
1	DABS transponder data interfaces	2
2	Timing convention for SM interface.	5
3	Timing diagram, SM interface	7
4	ELM interface.	13
5	Uplink data transfer	14
6	Downlink data transfer	16

SECTION 1 INTRODUCTION/SUMMARY

1.1 GENERAL

The transponder interfaces described here are intended to serve as a universal electrical connection between the transponder and the data input or output devices that are connected to it.

1.2 INTERFACE TYPES AND USES

Options for I/O devices associated with a DABS transponder range from a minimum of an IPC/PWI display to full Extended Length Message (ELM) handling equipment. The interface design reflects this flexibility. The Standard Message (SM) Interface is designed to handle single segment messages, either Comm-A alone, or both Comm-A and Comm-B. (Comm A is a ground-to-air communication transmission which includes a 56-bit communication message field; Comm-B is a similar transmission used in the air-to-ground communications [1]). The SM Interface is standard for all transponders and is capable of handling most ATC-related messages. In addition, transponders may be equipped with an Extended Length Message (ELM) Interface which can handle extended length messages and provides a standard I/O interface for available data terminals. Figure 1 illustrates the interface configuration.

1.3 SM INTERFACE

The SM Interface provides a "party line" type serial connection to and from data input and output devices which may be attached to the transponder. This line, designated the wire link, can also serve as an interface for ALEC readout and pilot acknowledgment.

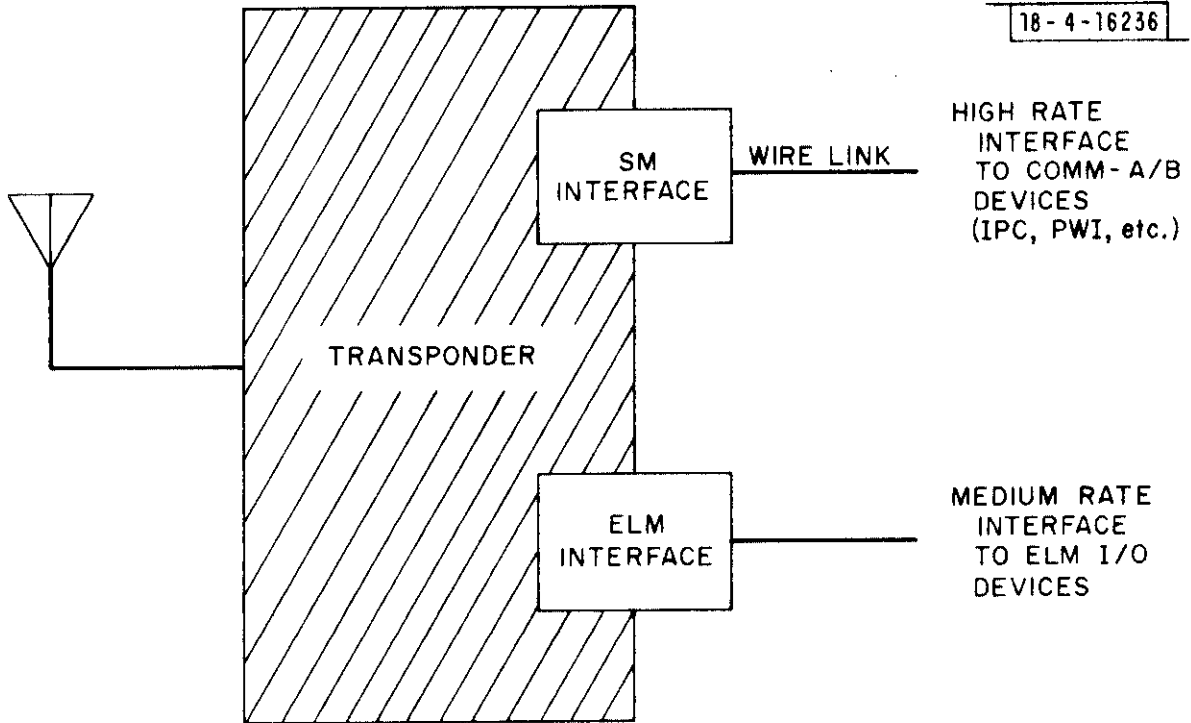


Fig. 1. DABS transponder data interfaces.

The interface employs a pair of lines; the data line, which operates serially in either direction at a 1 Mb/sec rate, and the clock line, which is used to synchronize transactions.

The information content of the DABS uplink transmission is transferred to the I/O devices before the downlink transmission begins. During the DABS downlink transmission, information is transferred from the I/O devices to the transponder for inclusion in the reply.

1.4 ELM INTERFACE

1.4.1 Uplink Transmissions

A transponder equipped for Extended Length Message operation will be capable of receiving, verifying, storing, and acknowledging an uplink ELM transmission. Following receipt of the entire ELM (as determined by the protocol described in Ref. [1]), the transponder transfers the entire ELM to an I/O device connected to the ELM interface. This transfer employs an uplink transfer clock line and an uplink data line to shift out serial binary data.

1.4.2 Downlink Transmissions

A downlink ELM transmission originates in an I/O device which assembles the message for transfer to the transponder. When a message is ready for transmission, the I/O device requests permission to transfer the data to the transponder. As soon as the transponder can accept the data it signals the I/O device, and the downlink message is transferred across the interface into the transponder. This transfer is done in a serial manner by means of downlink transfer clock and data lines. The subsequent transfer of the message from the transponder to the ground interrogator proceeds without further interaction with the I/O device.

SECTION 2

STANDARD MESSAGE INTERFACE

2.1 SIGNAL FLOW

After an uplink transmission has been received and verified, the information content of the transmission is shifted out at a 1 Mb/sec rate from the SM interface to peripheral devices. This process is finished before the transponder downlink transmission begins. At the time of the downlink transmission, data are shifted in on the data line at a 1 Mb/sec rate for direct insertion into that transmission. Two lines are used ^{to} accomplish this; the data line, operating in either direction and the clock line, which provides the necessary timing. Activity on the SM Interface takes place only during the interrogation-reply cycle of the transponder. It begins when the first clock pulse appears on the clock line and terminates after the last clock pulse has been sent out by the transponder.

2.2 ELECTRICAL INTERFACE

2.2.1 Logic Convention

The clock and data lines are symmetrical two-wire lines operating at TTL signal levels [3]. A high, or more positive voltage on the "true" wire and a low, or less positive voltage on the "complement" wire is interpreted as a logical "one." A low, or less positive voltage on the "true" wire and a high, or more positive voltage on the "complement" wire is interpreted as a logical "zero."

2.2.2 Clock Line

The clock line is a symmetrical line carrying the timing pulses for reference in data transmission. Line levels and impedances are those generated by a National Semiconductor DM 8831, or equivalent, operated in the differential mode. The signal on the clock line consists of a series of pulses occurring at a 1 Mb/sec rate. The pulse width is $0.5 \pm 0.1 \mu\text{sec}$. The number of clock pulses in each operational cycle is 214. When not active, the clock line is held low.

2.2.3 Data Line

The data line is a symmetrical data transmission line. Line levels and impedances are those generated by a National Semiconductor DM 8831, or equivalent, operated in the differential mode. The line has three states, HIGH, LOW, and OFF, to permit control by either the transponder or the I/O devices [4].

2.3 SM INTERFACE TIMING

2.3.1 Timing Convention

Events in the transponder are referenced to the time of the sync phase reversal in the DABS data block, or, for transactions involving the DABS/ATCRBS All-Call interrogation, referenced to the leading edge of the P_4 pulse. All events on the SM interface are referenced to the beginning of the first pulse on the clock line. As illustrated in Fig. 2, t_n is the instant in time at which the n th clock upstroke after the beginning of the clock cycle occurs. The time of the first upstroke is t_0 .

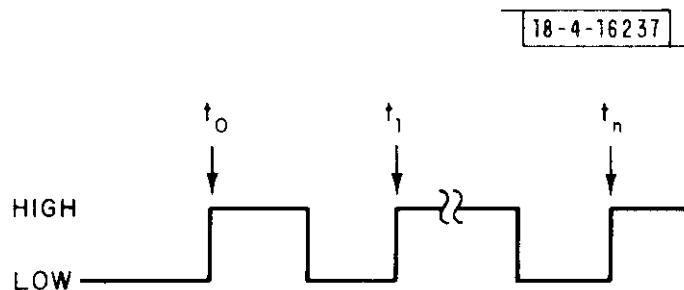


Fig. 2. Timing convention for SM interface.

2.3.2 Interface Initiation

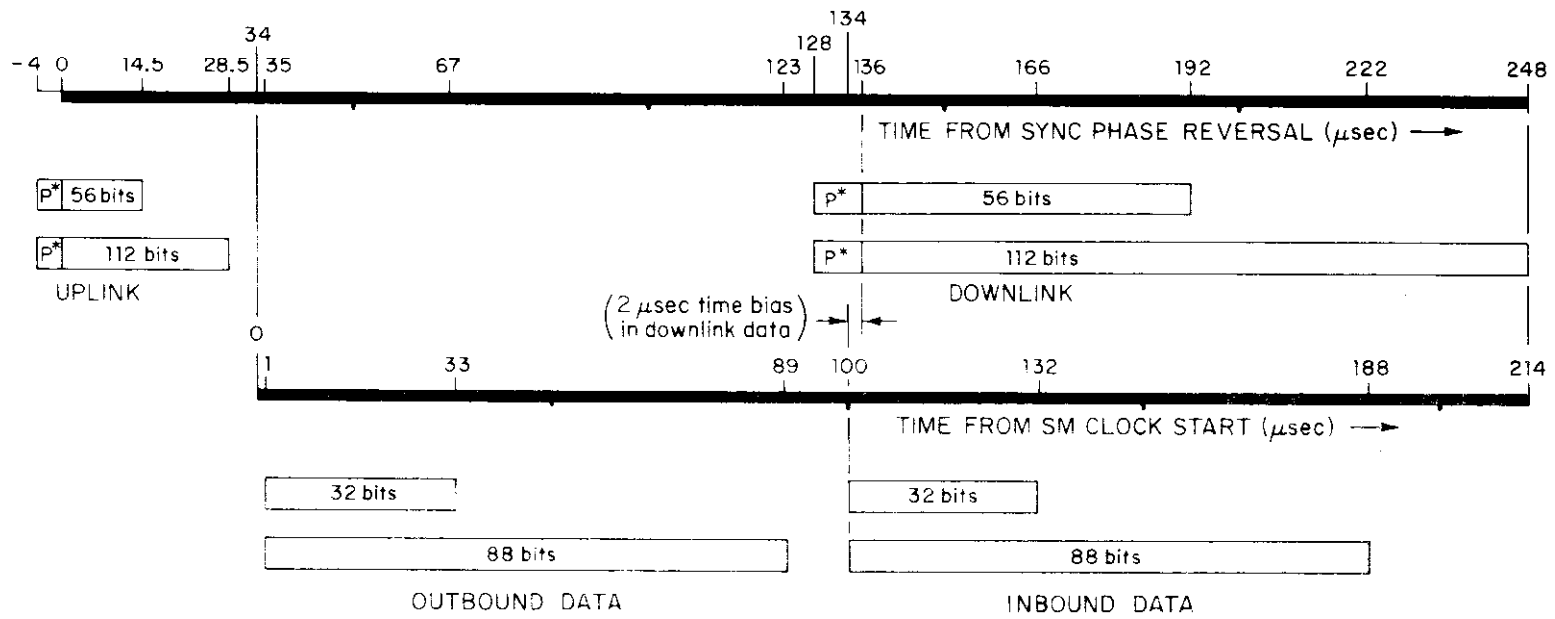
The first clock pulse starts (i. e., the SM interface becomes active) after the transponder has recognized a properly-addressed surveillance or Comm-A interrogation, an all-zero-address interrogation or an All-Call interrogation, provided the reply is not suppressed by a lockout state. (All-Call replies may be formulated from data received via the wire link, as discussed in Section 2.4.2, or from data hardwired to the transponder. In the latter case, the initiation of the wire link in response to an All-Call interrogation is not required.) The first clock pulse will start $34 \pm 0.05 \mu\text{sec}$ after either the sync phase reversal or the upstroke of P_4 .

2.3.3 Time and Level Assignments

When not active, the clock line is held low and the data line is left in the OFF state as defined in Section 2.2.3. When an interface transaction is initiated, the timing diagram of Fig. 3 and the event timing of Table 1 apply to all except All-Call interrogations. Use of the wire link in the formulation of All-Call replies is discussed in Section 2.4.2.

In the interval between t_0 and t_1 , the data line remains OFF. Beginning at t_1 , the complete information content of the uplink transmission, starting with bit 1 and ending with the last bit before the address-parity field, is impressed on the data line. The data line remains in the state (HIGH or LOW) of the first uplink information bit from t_1 to t_2 and then assumes the state of the next bit in the time between t_2 and t_3 , etc. This results in a non-return-to-zero format with a 1 Mb/sec data rate.

For a Comm-A interrogation, the data transfer terminates at t_{89} . If a surveillance interrogation is received, meaningful data end at t_{33} ; in this case, the transponder is permitted to generate either HIGH or LOW state signals on the data line between t_{33} and t_{89} . The I/O devices need not examine this interval because information about the length of the expected message is contained in bit 2.



P^* = PREAMBLE

18-4-16238

Fig. 3. Timing diagram, SM interface.

Beginning at t_{89} , the transponder relinquishes control of the data line by setting the line into its OFF state. At t_{94} , the transponder begins the downlink transmission. Downlink data transfer on the wirelink begins at t_{100} . The data bits are transferred to the transponder 2 μ sec before they are to be transmitted in order to provide an opportunity for proper strobing and synchronization. This feature is labeled "downlink data time bias" in Fig. 3.

Table 1. Relationship between uplink/downlink Timing and SM interface timing.

Event	Time From Sync Phase Reversal (μ sec)	Time From Clock Start (μ sec)
Start, uplink preamble	-4	-
Sync phase reversal	0	-
End, 56-bit uplink	14.5	-
End, 112-bit uplink	28.5	-
Start, SM clock	34	0
Start, SM data out	35	1
End, 32-bit data out	67	33
End, 88-bit data out	123	89
Start, downlink preamble	128	94
Start, SM data in	134	100
Start, downlink data	136	102
End, 32-bit data in	166	132
End, 56-bit downlink	192	158
End, 88-bit data in	222	188
End, 112-bit downlink	248	214
Stop, SM clock	248	214

The transponder assembles the downlink data stream from the data generated internally and from information supplied by the data line. Each input device contributes only the bit or bits which it is designed to handle by holding the data line either HIGH or LOW during the assigned time slot, and leaving the data line OFF at all other times. The I/O devices are addressed by uplink content or interrogation protocol so that only one device can occupy the data channel during the transmission time of a Comm B-downlink Message Field (MB).

In the time interval from t_{188} to t_{214} , the transponder generates the address-parity field. The SM interface clock continues to run during that interval.

2.4 PBUT AND CAPABILITY INTERFACE

There are two sources of PBUT and capability information available to the transponder: a serial source via the wire link, and a parallel source via direct connections. The transponder will accept information from either source and set the appropriate bits in the downlink transmission accordingly. In any given installation only one source of PBUT information and one source of capability information will be used.

2.4.1 PBUT Interface

It is anticipated that many transponder installations will not incorporate downlink message (Comm-B or D) capability. As an alternative to the bidirectional use of the data line in this case, two input terminals shall be provided at the transponder SM interface which receive signal levels representing the PBUT (pilot acknowledgement) code to be transmitted. The terminals are labeled Y (yes) and N (no) and represent bits 13 and 14 respectively, of the downlink transmission. The signals on the wires consist of standard TTL logic levels which change as required after receipt of the uplink but before the start of the downlink. The change will be complete by t_{92} . A high level indicates that the appropriate bit should be set.

2.4.2 Capability Interface

The transponder's All-Call reply includes the "Capability" field which describes the presence or absence of five data-accepting or generating I/O devices installed in the aircraft. One specific bit in the All-Call reply is assigned to each device and a sixth bit indicates the presence of additional devices whose identity can be ascertained by the sensor by means of a special Comm-B interrogation. Bit assignments are given in Ref. [1].

The capability code is entered into the transponder either through a hardwired connection to the capability connector or through the wire link. The hardwired connector is provided for use in installations which do not have wire link capability-code operation. Installations which have wire link capability-code operation will normally not use the hardwired capability-code connector, as the use of wire link alone provides automatic elimination of a capability code bit when a given peripheral is disconnected or turned off.

The operation of the wire link capability code reporting is as follows: A valid All-Call can be received either as a DABS/ATCRBS All-Call interrogation or as a DABS-only All-Call interrogation. In either case, the wire link will be initiated as described in Section 2.3.2. Receipt of a valid DABS-only All-Call will result in the transfer of the received data block over the wire link. The first bit (F) of the data block is a logical one in an All-Call interrogation [1].

If a valid DABS/ATCRBS All-Call is received, the transponder holds the data line high between t_1 and t_2 , thereby creating an $F=1$ condition in the wire link data. The transponder then holds the data line in one of the ON states up to t_{89} .

Peripherals will recognize that an All-Call has been received in either case because all other patterns allowed on the wire link begin with a logical zero between t_1 and t_2 . A given peripheral indicates its presence by holding the data line HIGH at its assigned time slot between t_{102} and t_{108} . Peripherals, other than the five specified in Ref. [1], set the sixth bit. In this manner, a disconnected or malfunctioning peripheral does not report its presence and I/O device installation changes can be made without disturbing the transponder.

SECTION 3 ELM INTERFACE

3.1 ELM SIGNAL FLOW

3.1.1 Uplink

Immediately following receipt of a complete ELM, as indicated by the successful receipt of all segments, the transponder activates its output transfer clock and its data output signal lines. The contents of the MC fields are shifted out of the transponder in a serial bit stream on the data line, starting with bit 1 of segment number one and ending with bit 80 of the highest segment number used. Segment numbers are not shifted out. The output data appear as a continuous bit stream for the duration of the ELM. The transponder will not accept a new uplink ELM until it has shifted out a previous ELM.

3.1.2 Downlink

Downlink ELM's are generated in the I/O devices. When an I/O device has a message to be transmitted, it signals the transponder with a "Request to Send" signal. When the transponder is ready to accept downlink data, it answers with a "Clear to Send" signal. The I/O device then commences to transfer data to the transponder in a continuous serial bit stream for the duration of the ELM. As it receives the data, the transponder divides it into 80-bit segments, assigns segment numbers to each segment, and stores the information.

The end of the ELM is signalled by the end of the "Request to Send" signal. In the event the I/O device attempts to load a message in excess of the maximum length of one ELM (1280 bits), the message will be terminated at that point by the transponder through resetting of the "Clear to Send" signal.

Following the transfer of an ELM from the I/O device to the transponder, the transponder requests permission to transmit it to the ground. The request and subsequent operation of the transponder are described in Ref. [1].

3.2 ELM ELECTRICAL INTERFACE

3.2.1 General

The ELM interface has been configured in accordance with the Electronic Industries Association (EIA) Standard RS-232C [2]. The provisions of that Standard apply unless specifically stated otherwise herein.

3.2.2 Data Transfer Rate

The ELM electrical interface operates in a full duplex mode to receive data from, and transfer data to, one or more I/O devices. The data transfer rate is fixed at 2400 b/sec, controlled by a clock located in the transponder.

3.2.3 Signals

A block diagram of the ELM interface is shown in Fig. 4. The interface is configured using signals defined in RS-232C (Interface Type D). The signals used are shown in Table 2. The electrical characteristics of the signals at the interface are described in detail in Ref. [2]. Signal CC, "Data Set Ready," is connected to the "Standard"-DABS contact circuit in the transponder, and serves to signal the I/O device when a ground-to-air communication link exists.

3.3 ELM INTERFACE TIMING

3.3.1 Uplink Interface

The received data are shifted from the transponder to the I/O devices by means of the "Received Data" signal and the "Receiver Signal Element Timing," transfer clock signal. The clock and data appear simultaneously on their respective lines as shown in Fig. 5. The ON to OFF transition of the clock occurs at the midpoint of the bit interval. The clock signal is present only for the duration of the message.

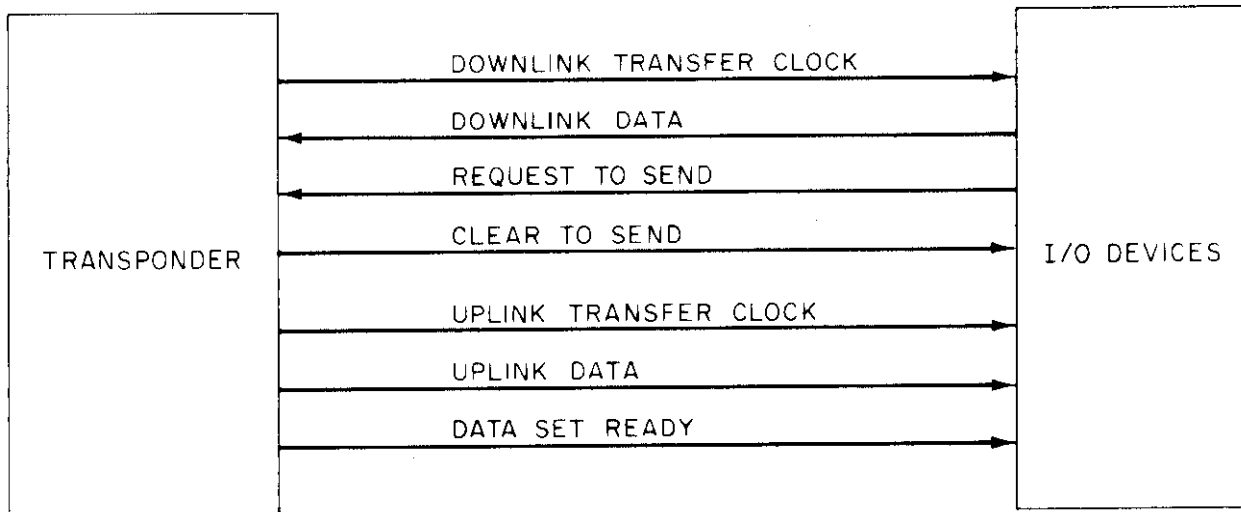
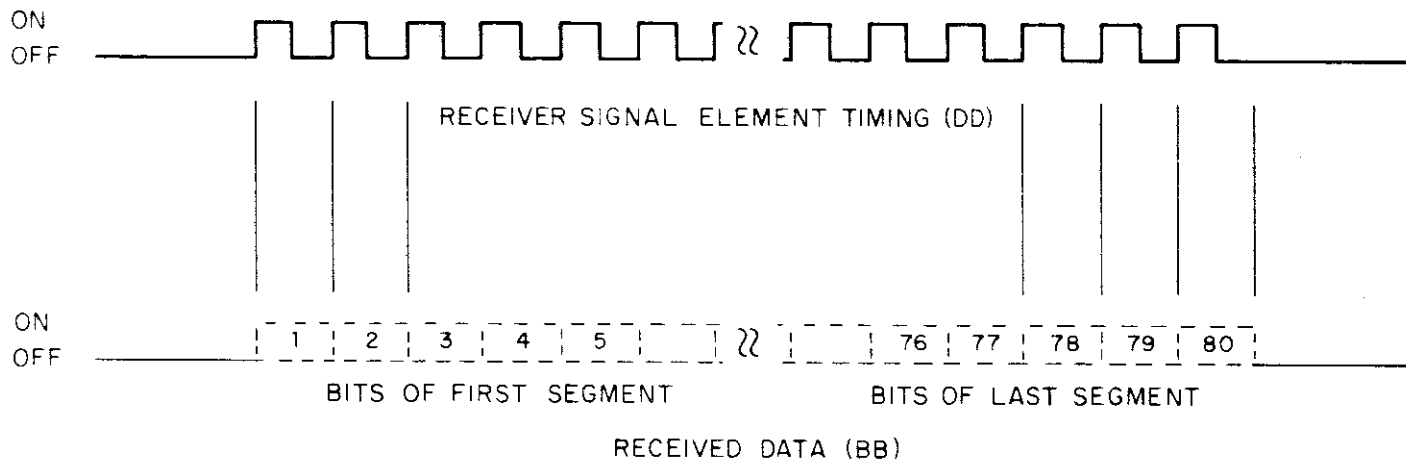


Fig. 4. ELM interface.



14

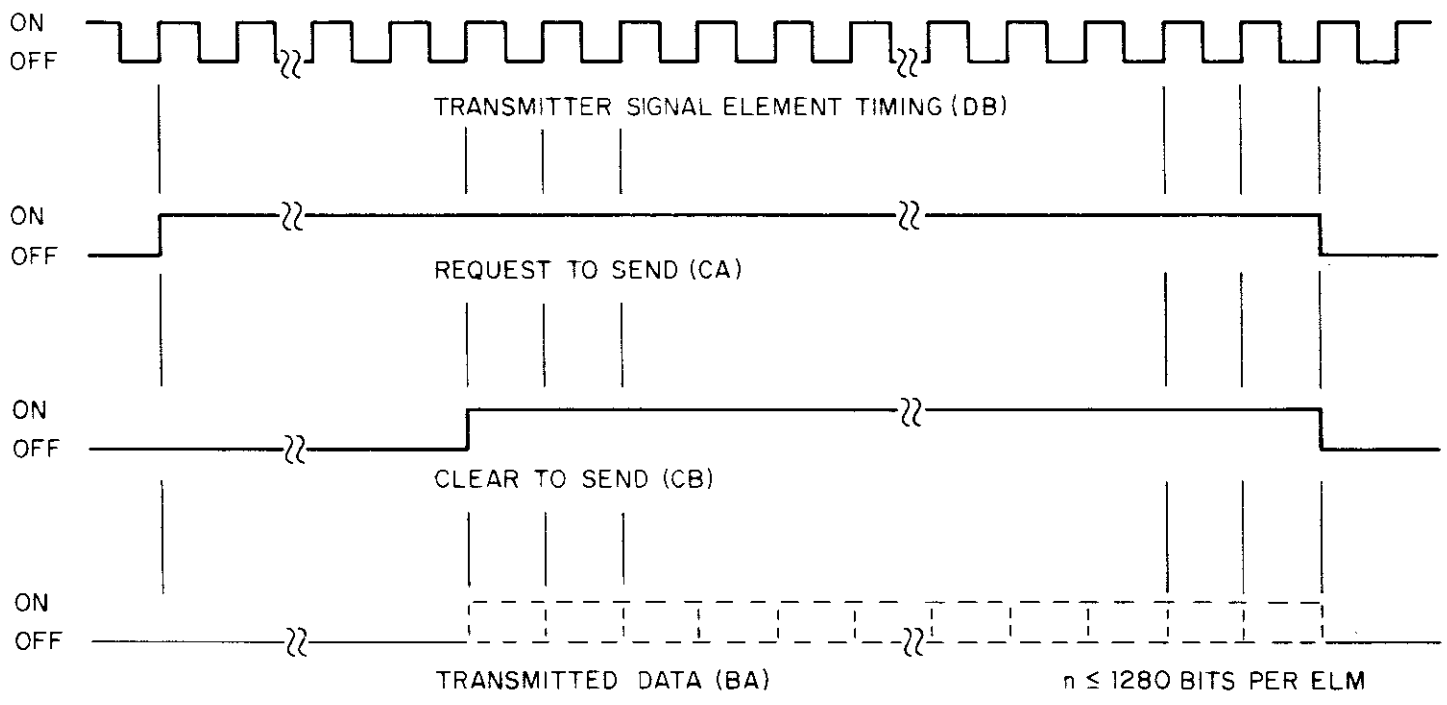
Fig. 5. Uplink data transfer.

Table 2. Signal names and functions.

Function	RS-232C Name
Uplink transfer clock	DD Receiver Signal Element Timing
Uplink data	BB Received Data
I/O request to send	CA Request to Send
Transponder OK's to send	CB Clear to Send
Downlink transfer clock	DB Transmit Signal Element Timing
Downlink data	BA Transmit data
Indicates "Standard" DABS contact.	CC Data Set Ready

3.3.2 Downlink Interface

The "Transmit Signal Element Timing" downlink transfer clock normally runs at the 2400 b/sec rate and is always available at the interface. (RS-232C allows the clock to be stopped infrequently for short periods to accommodate test modes, etc. No transfer is allowed unless this clock is running, and conversely, the clock remains running throughout a transfer.) The I/O device generates a "Request to Send" signal whose OFF to ON transition coincides with that of the clock, as shown in Fig. 6. When the transponder is ready to accept data it replies with a "Clear to Send" signal whose OFF to ON transition also coincides with that of the clock. The I/O device immediately makes downlink data available to the transponder. The ON to OFF transitions of the clock coincide with the midpoints of the bit intervals. The end of "Request to Send" coincides with the end of the last data bit interval, and causes "Clear to Send" to end also.



16

Fig. 6. Downlink data transfer.

REFERENCES

- [1] P. R. Drouilhet, Ed., "Provisional Signal Formats for the Discrete Address Beacon System," Project Report ATC-30, Rev. 1, Lincoln Laboratory, M.I.T. FAA-RD-74-62 (25 April 1974).
- [2] EIA Standard, "Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange," RS-232-C, Engineering Dept., Electronics Industries Assoc., (August 1969).
- [3] "The TTL Data Book for Design Engineers," Texas Instruments Incorporated, (1973).
- [4] "Digital Integrated Circuits," National Semiconductor Corporation, Santa Clara, California, p. xii (1971).